FARADAY

Selanar 100XL™ Graphic Terminal

Maintenance Manual

FARADAY

CORPORATE HEADQUARTERS
Faraday Electronics, Inc.
749 North Mary Avenue
Sunnyvale, CA 94086
408-749-1900 Telex 706738
FAX #408-738-1671

EUROPEAN HEADQUARTERS
Faraday Electronics Ltd.
Technology House
Easthampstead Road, Bracknell
Berkshire, RG12 1LX, England
Telephone 0344 486677
Telex 847096 EMDAL
FAX #44 344 485210

Selanar 100XL™

Maintenance and

Troubleshooting Manual

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749 North Mary Avenue
Sunnyvale, California 94086
408-749-1900 Telex 706738
FAX #408-738-1671

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Section A

HiREZ 100XL Theory of Operation

1.0 6809 Microprocessor and BUS

The Motorola 68B09E is an 8 bit microprocessor with a 16 bit internal architecture. Its sixteen address lines are buffered using two 74LS244s to provide greater fan-out. Its eight data lines are buffered using a 74LS245 bi-directional buffer. The processor runs at 2 MHZ provided the character FIFO (explained later) is in its quiescent state; otherwise it may be held. The processor has three general purpose interrupt request inputs: 'IRQ', 'FIRQ', and 'NMI', in order of lowest to highest priority. Interrupts are generated under the following conditions:

'IRQ': AUX UART #1 has received a character
AUX UART #1 is ready to transmit a character
AUX UART #2 has received a character
AUX UART #2 is ready to transmit a character
Screen refresh is about to begin (real time clock)

'FIRQ': CPU UART has received a character
CPU UART is ready to transmit a character

'NMI': Keyboard serial data communication is about to commence

1.01 BUS Device Selection

BUS device selection is handled by a PAL12L10 (U88) programmable logic array. This device decodes the processor address BUS and provides chip select signals to all devices on the BUS except screen RAM.

1.02 Program Memory

The HiREZ 100XL has the capability to address up to 56K of program memory, bank switched in two sections of 28K. The current implementation uses all 28K of the primary section ('Bank' = 0), and 8K of the secondary section ('Bank' = 1). In order to switch between banks the processor must execute a piece of code which occupies the same address location in both banks. This piece of code will toggle the 'bank' bit (WREXT REG, Bit 5) thereby continuing program execution in the opposite PROM bank.

1.03 Scratch RAM

The HiREZ 100XL has 2K of CMOS static RAM, which is battery backed up. When power is on, +5V is supplied to the RAM through diode CR3 and the RAM chip select line is passed through transistor Q3. When power is switched off, current from the battery is supplied through diode CR3 and as +12V begins to drop, the zener diode (CR1) voltage drops, thus Q3 stops conducting as the base voltage is turned off.

1.04 UARTS and Serial Ports

There are three 6551A-1 UARTs in the HiREZ 100XL, one for CPU communications and two for auxiliary ports. The AUX port #1 UART doubles as a real time clock generator. An interrupt is generated on every edge of 'RAO' (16 MS).

1.05 CRT Controller

The 68B45 CRT controller generates HSYNC, VSYNC, and display enable. Graphics RAM vertical addresses are generated by PAL 20X10 (U48) used as a 9 stage counter. The character generator horizontal addresses are generated by a 74LS393 (U65) 8 stage counter.

1.06 'IOCTL' Register

The 'IOCTL' register (U56) is a write only output register from the BUS. Its outputs are defined as follows:

Bits 0-3	Brightness	0 = Brightest	F = Dimmest
Bit 4	24/48	0 = Line Mode	1 = 24 Line Mode
Bit 5	80/132	0 = 132 Column Mode	1 = 80 Clmn Mode
Bit 6	Blink Freq	Blink Attribute Control	
Bit 7	NMI Hold	0 = Holds NMI Low for Keyboard Communication	

1.07 'BITADD' Register

The 'BITADD' register (U53 and U54) is a read/write I/O register on the BUS. Its outputs are defined as follows:

Bit 0	Keyboard I/O pin
Bit 1	Word address mode; a write occurs in all 16 dynamic RAMs when this pin is high. Used for clear screen.
Bit 2	Byte address mode; a write occurs in the selected eight RAMs when this pin is high. Used for data storage.

Note: When the previous two pins are low, 'bit address' mode exists and only one RAM will be written to at a time. Used in drawing graphics.

Bits 3-7	Bit addresses BA0-BA4; these lines should be considered as the least significant graph RAM addresses.

1.08 'WREXT' Register

Bits 6-7	Graphics plane to be displayed (valid only when 256K RAMs installed)		
Bit 5	PROM bank select	0 = Primary	1 = Secondary
Bit 4	Graphics video on flag	0 = OFF	1 = ON
Bit 3	Character video on flag	0 = OFF	1 = ON
Bit 2	Graphics/Character RAM select	0 = CHAR	1 = GRAPH
Bits 0-1	Graphics plane to Read/Write (valid only when 256K RAMs installed)		

1.09 Screen RAM Bank Control Logic

The screen RAM is organized in two major blocks, graphics RAM and character RAM. The graph RAM (unexpanded) is organized as four blocks of 32K bytes each. The character RAM is organized as one block of 32K bytes. All five of these 32K blocks of memory can be mapped into the lower 32K of the processor's address space. This mapping operation is controlled by a PAL10LB (U72). This device decides, based on A15 and R/W, which bank should be selected and when. It also decides when to hold the processor, based on the status of the character RAM FIFO. When the FIFO is in 'catch up' mode and the processor is requesting access to character RAM, the -Hold output is dropped causing E and Q clocks to stop. When the processor switches from character to graph RAM address mode, the E and Q clocks must be re-synchronized to the dynamic memory system. This is done by holding E and Q for the amount of time required.

1.10 Memory Map

Address (in HEX)	Function
FFFF-9000	Program PROM space, bank switched
8880	Bitadd Register
8860	WREXT Register
8840	IOCTL Register
8833	AUX Port #2 UART Control Register
8832	AUX Port #2 UART Command Register
8831	AUX Port #2 Status/Reset Register
8830	AUX Port #2 Data Register
882B	AUX Port #1 Control Register
882A	AUX Port #1 Command Register

8829	AUX Port #1 Status/Reset Register
8828	AUX Port #1 Data Register
8827	CPU Port Control Register
8826	CPU Port Command Register
8825	CPU Port Status/Reset Register
8824	CPU Port Data Register
8801	CRT Controller Data Register
8800	CRT Controller Address Register
87FF-8000	Scratch RAM
7FFF-0000	Screen Ram, Graph RAM, Character RAM

2.0 Main System Timing

All clocks in the HiREZ 100XL, except for baud clock, are derived from the 32 MHZ oscillator chip (U9). This clock is divided into 16 states by U11. These states, defined by P0, P1, P2, and P3, are decoded into all other system clocks. E and Q clocks are the main processor clocks; all data transfers into and out of the processor are done on the negative edge of E clock. Q clock is simply a quadrature of E clock.

2.01 E and Q Clock Generation

E and Q clocks are generated with two D-type flip-flops (U62), one generates E and the other generates Q. These two flip-flops are set up such that E will always follow Q, one quarter E cycle later. Both flip-flops are clocked by P1 clock, gated with -Hold. This provides one full E clock cycle every 16 dot clocks, provided the -Hold signal stays high for the duration. When accessing graph RAM after accessing character RAM, E and P3 clocks must be synchronized to allow proper access to graph RAM.

2.02 Dynamic Memory Timing

Dynamic memory timing consist of three signals: -RAS, COL/-ROW, and -CAS. -RAS is a quadrature of P2. COL/-ROW is -RAS delayed by 31.25 NS. -CAS is inverted P2. Given these three signals, dynamic memory timing can be summerized as follows: the processor address BUS becomes stable, @ 60 NS later -RAS drops, latching the eight least significant address lines, 31.25 NS later COL/-ROW raises to select the most significant 8 addresses, 31.25 NS later -CAS drops, latching the most significant addresses. @ 90 NS later data should be valid on the RAM outputs. This data will either be asserted onto the data BUS or clocked into the graph video shift registers. Dynamic RAM refresh is handled inherantly by the CRTC screen refresh. The least significant eight screen address lines are used for the ROW addresses, hence the entire RAM is refreched in two HSYNC times.

3.0 Bit Mapped Graphics System

Bit mapped graphics is configured from sixteen 64K 4164-12 type DRAMS memory. Each bit in these RAMs corresponds to one dot on the screen. The processor can write to these RAMs in one of three modes: word address mode, byte address mode, and bit address mode. In word address mode, all 16 RAMs are written to simultaneously with data on the data BUS. This mode is used primarily for fast clear screen. In byte address mode, only the selected 8 bits are written to from the data BUS. This mode allows the processor to use available excess dynamic memory as standard scratch RAM, primarily for vector storage. In bit address mode, only one selected bit is written from the data BUS. This mode is used in drawing graphics. The 16 individual RAM write pulses are generated by 2 PAL16R8s (U51 and U52). Due to an arbitration scheme known as clock interleaving, both the processor and the CRT controller have 100% access to dynamic RAM. When E clock is low, the processor does not use the BUS. At this time, the CRTC addresses are asserted to the dynamic RAMs. The screen refresh data are clocked into the shift registers at the same time as E clock is driven high. At this time, the processor is given full access to the RAM. For this reason, the dynamic RAMs must have a cycle time of 250 NS or less (E clock freq.*2) and an access time of 120 NS. Once the RAM data is clocked into the graphics video shift registers, it is shifted out serially, one dot every dot clock, thus converting parallel RAM data into serial video data.

4.0 Character Generator System

The character generator is composed of 16 2K RAMs (8 for character data and 8 for attribute data), 2 8K character generator PROMs, and a 16 bit wide shift register, all tied together by a three stage FIFO system. The character address space is organized as 64 lines of 256 characters each.

4.01 Character and Attribute

There are 32K bytes of static RAM, 16K for character storage and 16K for attribute storage. The processor accesses this RAM as one 32K block of memory. The character plane occupies addresses 0000-3FFF (HEX), attribute plane occupies addresses 4000-7FFF. During screen refresh, both of these 16K planes are accessed simultaneously. The 8 bits of character data are sent to the character generator PROM to select one of 256 dot patterns. The 8 bits of attribute data are distributed throughout the logic to generate the various character attributes as explained later.

4.02 Character Generator FIFO

Due to the fact that the character generator timing must be variable (based on character width), the clock interleaving arbitration scheme used in accessing graph RAM cannot be implemented for character RAM. For this reason, a three stage FIFO scheme is used to arbitrate processor and screen refresh cycles. Normally, the screen refresh circuitry has full access to RAM and all three FIFO stages are kept full. When the processor needs access to RAM, it asserts the proper address to the bank control logic, which will wait until the first stage of the FIFO completes its current cycle; the processor will be held if necessary. At the end of the current 1st stage cycle, the FIFO will relinquish the character RAM BUS to the processor, during which time the contents of the FIFO will be emptied to

video shift register at the proper speed to guarantee un-altered screen refresh. At the end of the processor cycle, the bank control logic dispatches a signal called '-restore' which indicates to the FIFO that the processor is finished with the BUS. The FIFO regains the BUS and proceeds to fill itself back up as quickly as possible. It is also the FIFO's responsibility to maintain memory access times and latch propagation delays. The first stage takes care of latching data outputs from character RAM to character PROM. It guarantees a minimum of 200 NS access time. The second stage takes care of latching data from characteer PROM to the shift registers. It also guarantees an access time of 200 NS. The third stage is basically a variable delay timer which is used to load the shift registers. In 80 column mode, it loads them every 8 dot clocks.

4.03 Character Generator PROM

Character RAM data is latched into a 74S374 (U66) by the FIFO 1st stage. The outputs of this latch are used to lookup the proper character dot patterns from the character PROMs (U20 and U44); these lines are used as addresses A4-A11. Addresses A0, A1, A2, and A3 are encoded from the row address lines based on the 24/48 line flag and on the double high attribute. The 80/132 column flag is used for the most significant character PROM addressing scheme can be summarized as follows: the row address lines RA0-RA4 generated by the CRTC are encoded into an absolute character row address, allowing selection of one of sixteen possible 16 bit dot patterns. The latched data from the character RAM is used to select between the two different character sets.

4.04 Character Video Shift Register

The sixteen bit character PROM output is latched into two 74S274s (U19 and U43) by the FIFO second stage. The character pattern data is now ready at the video shift register parallel input lines. The shift registers will be loaded by the FIFO third stage. The shift registers are normally clocked by dot clock. When drawing a double wide character, they are clocked by one half dot clock frequency.

4.05 Attribute Generator

All character attributes except double high and double wide are processed by a PAL18L4 (U36). Inputs can be broken into three groups: character and graphics video inputs, attribute information, and video gating signals. Attribute information includes underline, reverse video, bold, blink, and blink frequency. The encoded row address lines are used to generate the underline attribute. The video gating signals include character and graph video on/off flags, -VBLANK, character display enable, and graph display enable. Outputs include -video out, -bold out, and half intensity out.

5.0 Keyboard

All data transferred between the main processor and the keyboard processor is done so across a bi-directional serial link. Data is sent to the keyboard in the form of time encoded pulses, the length of which determines which one of three functions is to be performed. The available functions are as follows: perform a keyclick, perform a bell tone, or scan keyswitch matrix and report status back to main processor. When a scan matrix command is received by the keyboard processor, it responds by sending one 10 bit serial data word per key depressed, plus one more 10 bit serial word used as a terminator.

5.01 Communication from Logic to Keyboard

The main processor can request that the keyboard perform one of the functions outlined above by holding the serial I/O line low for a specified period of time. An interrupt will be generated in the keyboard processor when the I/O line drops, causing it to execute a special section of code. This code will time the incoming pulse and execute the proper function. If the pulse is less that 37.5 uS, it is interpreted as a glitch and ignored. If the pulse is between 37.5 and 75 uS, it is interpreted as a keyclick command. If the pulse is between 75 and 112.5 uS, it is interpreted as a bell command. If the pulse is greater than 112.5 uS, it is interpreted as a matrix scan command.

5.02 Communication from Keyboard to Logic

When requested to scan the keyswitch matrix, the keyboard processor will send a series of 10 bit serial data words, separated in time by at least 110 uS. One 10 bit word will be sent for each key down, plus a one word terminator. These data words consist of the following information: 4 bit row identifier, 3 bit column identifier, 2 bit status code, and 1 bit for the fast repeat key. The terminator work is identical to standard data words except for the fact that the row identifier has a value greater than eleven. Since there are only 12 rows, a row identifier of 12 or greater would otherwise be undefined. The terminator word will always be sent at the completion of a matrix scan, regardless of whether a key is pressed or not. The serial data format and bit times are outlined below.

5.03 Serial Keyboard Data Timing

Bit 9:	Status Code S0 (see below)
Bit 8:	Status Code S1 (see below)
Bit 7:	Fast Repeat, 1 = Fast Repeat Condition
Bit 6:	Row Identifier Bit 3 (MSB)
Bit 5:	Row Identifier Bit 2
Bit 4:	Row Identifier Bit 1
Bit 3:	Row Identifier Bit 0 (LSB)

Bit 2:	Column Identifier Bit 2 (MSB)
Bit 1:	Column Identifier Bit 1
Bit 0:	Column Identifier Bit 0 (LSB)

Status Codes	S1	S0
Normal Operation	0	0
Caps Locked	0	1
Shift Pressed	1	0
Control Pressed	1	1

Serial Data Word Format and Timing:

Start Bit	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	40 uS			20 uS						

5.04 Logic Received Data Processing

The main processor receives and de-serializes the keyboard data directly, eliminating the need for a UART. The keyboard input (KEYIN) is tied to two parts of the main logic: the processor 'NMI' line and to one input of an octal buffer, which allows a path to data BUS bit zero. The serial data start causes an NMI to occur in the main processor code. This code first drops the 'NMIHLD' line low, which will keep multiple NMIs from occurring during keyboard read. It then begins to sample the 'KEYIN' bit at fixed 20 uS intervals in order to convert the serial bit stream to parallel. After all 10 bits are read the data is converted to ASCII and placed in the keyboard buffer. The 'NMIHLD' line is set back high to enable future interrupts. Processing is then continued from the location where interrupt originally occurred.

5.05 Logic Transmit Data Processing

Commands are sent to the keyboard every 16.4 MS. If there is no bell command pending, a scan matrix command will be sent. Since the keyboard will never send data without being asked to do so, there can never be any data collision on the serial I/O line. The main processor sends commands to the keyboard by setting the 'KEYOUT' line high for a specified duration. This will cause negative pulse on the keyboard serial I/O line. This pulse will cause an interrupt to occur in the keyboard processor and timing loops are again used to decode the meaning of the pulse.

Section B

Terminal Checkout

Testing Procedures

The HiREZ 100XL has several built in diagnostic routines which allow testing and troubleshooting of the following sub-systems:

I/O Ports (CPU, AUX1, AUX2)

Graphics RAM

Character RAM

Scratch RAM

Screen RAM

Screen FIFO

Attribute Generator

Furthermore, there are two types of video test patterns for adjusting screen alignment.

Power Up Diagnostics

The HiREZ 100XL logic board, on power up, tests all onboard RAM and responds to a RAM fault in the following manner:

Scratch RAM Fault	The processor will continuously read and write to bad location, which will be readily apparent as a steady stream of pulses at the RAM chip select line.
Graphics or Character RAM	The HiREZ 100XL will send a failure report out through AUX port #1 at 9600 baud. One stop bit, 8 data bits, no parity. The message will outline the nature of the failure (bank, address, bit number).

If all power-up self tests pass, then no action is taken.

Callable Diagnostics

In addition to the power-up diagnostics, the HiREZ-100XL has a number of user callable hardware diagnostics. To execute these diagnostics, the terminal must be in "ANSI" mode, on-line, and have installed a "D-TYPE" RS-232 connector (female) at the CPU serial port, with pin 2 shorted to pin 3 and pin 20 shorted to pin 25. The tests and corresponding command sequences are as follows:

CPU Port Data Loop Test Type: esc [2 ; 2 y

In this test, data is sent out through the CPU I/O port. The same data is expected to be received a moment later or an error is reported.

Repeat Power-Up Process Continuously Type: esc [2 ; 9 y

Executes a full power-up initialization sequence continuously until failure.

Continuous CPU Port Data Loop Test Type: esc [2 ; 10 y

Performs CPU data loop test continuously until failure.

Auxiliary Port #1 Data Loop Test Type: esc [2 ; 16 y

Performs a data loop test on AUX port #1. A data loopback connector, as described in callable diagnostics, above, must be attached to AUX port #1 to perform this test.

Auxiliary Port #2 Data Loop Test Type: esc [2 ; 17 y

Performs a data loop test on AUX port #2. A data loopback connector, as described in callable diagnostics, above, must be attached to AUX port #2 to perform this test.

Continuous Aux Port #1 Data Loop Test Type: esc [2 ; 24 y

Performs AUX port #1 data loop test continuously until failure.

Continuous Aux Port #2 Data Loop Test Type: esc [2 ; 25 y

Performs AUX port #2 data loop test continuously until failure.

Screen Ram Test Type: esc [2 ; 50 y

Tests the character and graph RAM by writing a random pattern into memory, waiting 2 MS to test refresh, then verifying that the pattern still exists. A report will be sent to the screen whether RAM passes or fails. This test is performed in *local* mode.

FIFO/Attribute Test 80/24 Type: esc [2 ; 51 y

Draws all characters and attributes in 80 column by 24 line format. It then accesses the character RAM at very high speed to test FIFO recoverability. This test is performed in *local* mode.

FIFO/Attribute Test 132/48 Type: esc [2 ; 52 y

Draws all characters and attributes in 132 column by 48 line format. It then accesses the character RAM at very high speed to test FIFO recoverability. This test is performed in *local* mode.

Continuous RAM and Data Loop Tests Type: esc [2 ; 53 y

Performs screen RAM test and all data loop tests continuously until failure. Test results are reported to screen.

Section C

Troubleshooting Procedures

The following Troubleshooting information will help to pin-point and diagnose faults on the HiREZ 100XL logic board.

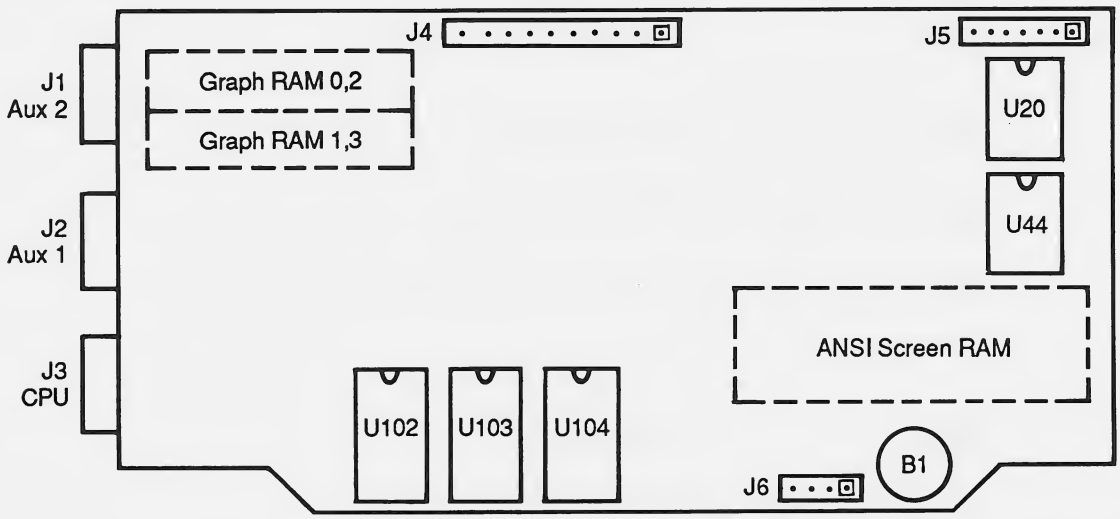


Figure 1. Board Layout

U20, U44 = Character Proms
U102, U103, U104 = Control/Printer Proms

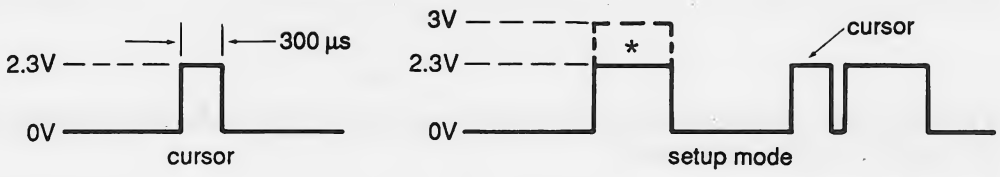
Power Connector - J4:

Pins 1&2	+12 VDC
Pins 5,6,&7	5VDC
Pins 3,4,8&9	GND
Pin 10	-12 VDC

All voltages are +/- 5%

Video Connector - J5:

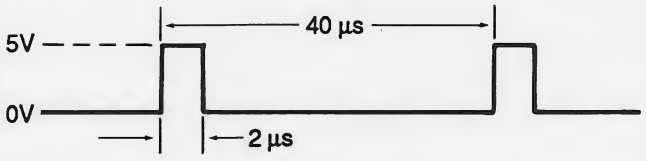
Pins 1,4,&6 Ground
Pin 5 Video



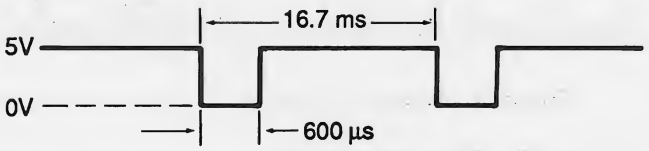
*Setup menu single/double intensity

Pin 7 +12 VDC

Pin 2 Horizontal Sync



Pin 3 Vertical Sync

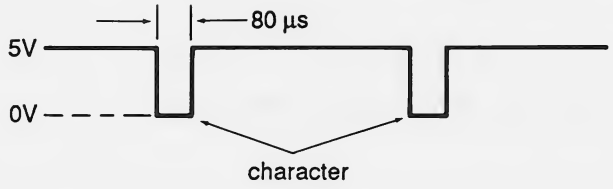


NVR Circuit: (Non-Volatile RAM)

The NVR battery back-up (B1) is lithium and should be approximately +3 VDC. The circuit should also be checked during power-down by monitoring U101, pin 18 which should be +3 VDC +/- 10%.

Keyboard Connector - J6:

Pin 1 Keyboard I/O (Time Base = 200 MS)



Pins 2, 4	GND
Pin 3	~12.0 VDC

Power-Up:

The power-up sequence for the XL is as follows:

1. Keyboard "beeps" - Power supply and keyboard powered-up successfully.
2. Character and Graphics RAM are tested - low intensity video is displayed on screen.
3. Second keyboard "beep" - logic board completed self-test successfully.
4. Cursor appears on screen - video is turned on.

The following steps may be used as a guide to isolate failures to the appropriate sub-assembly.

Failure	Possible Causes
No initial beep	- AC line fuse blown - Internal power supply fuse blown - Bad power supply - Keyboard not plugged in
No final beep	- Logic board failed to complete power-up self test - Terminal needs Default parameters set (Select Setup, shift D/S, reset)
No Video	- Logic board failure - CRT Monitor assy. - Terminal needs Default parameters set (Select Setup, shift D/S, reset)
Two beeps after initail keyboard beep	- RAM failure in self test (Terminal will still power-up)

Failure Diagnosis - Logic Board:

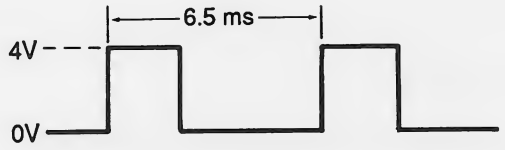
Failure to complete self-test on power-up can be isolated as follows:

1. Check clock signals:

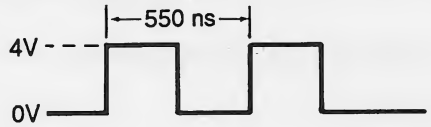
a. 32 MHZ on U11-2 and all DOT and DOT 0 signal lines.
b. 2 MHZ on P3 signal lines.
c. 4 MHZ on P2 signal lines.
d. 8 MHZ on P1 signal lines.
e. 16 MHZ on P0 signal lines.

2. On power-up check:

a. U83-5



b. U83-6 (baud rate clock)



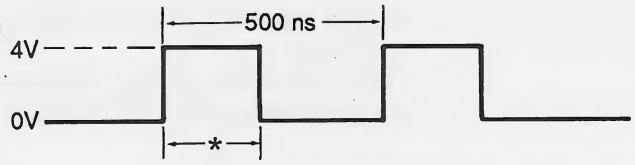
3. No video:

Check R14 - should be 10VDC at maximum intensity.

4. Extraneous video: (ANSI mode)

Check:

a. RAS and CAS signals are present.
b. U46-2 (same as RAS/CAS)
c. U46-14



**PW will decrease as follows and then repeat: 250 NSEC, 125 NSEC, 120 NSEC, 0 NSEC*

5. Special Note: For logic boards with part number 900-0004 up through revision A11.

   If there are:

a. Extraneous dots in graphics
   Verify update to revision release A11, or
   Verify a 3-wire modification on U37.
   Verify PAL piggyback in place of 4040 (PAL 20X10).

b. "Snowy" characters
   Verify update to revision release A11, or
   Verify a 2-wire modification on U61.

c. Missing portions of characters
   Verify update to revision release A11, or
   Verify a 3-wire modification on U57
   or
   Character Proms U20 and U44 reversed.

Section D

CRT Display Adjustment

Following rework or sub-assembly replacement, adjustment/alignment may be required. All are done with the terminal in LOCAL/ANSI mode, 80 characters per line, unless otherwise noted.

Video Monitor Board

Remove the monitor cover by removing the two (2) phillips screws located on the underside of the upper case and then sliding the cover straight back.

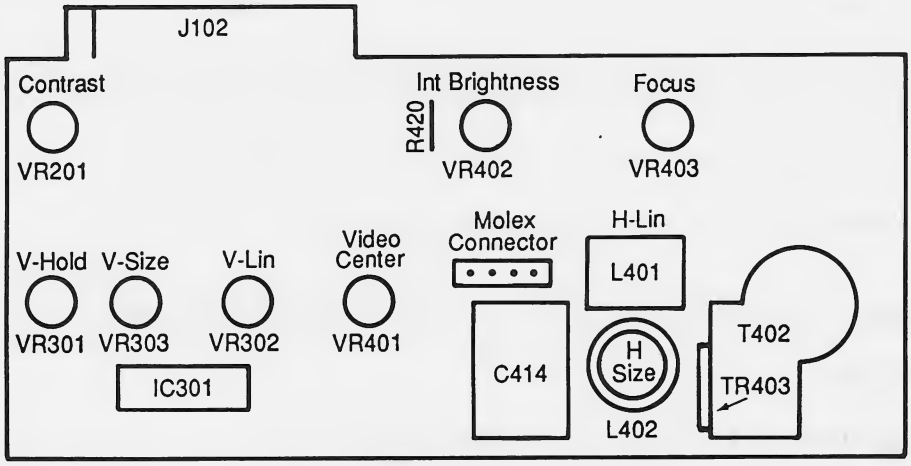


Figure 2. Monitor Board Layout (Top View)

Adjustment Components:

VR201	Internal Contrast
VR402	Internal Brightness
VR403	Center focus
VR301	Vertical hold
VR303	Vertical size
VR302	Vertical linearity
VR401	Video center
L402	Horizontal size
L401	Horizontal linearity

Connectors:

J102 = video information from Logic board connector J5.

J103 = Horizontal/Vertical Deflection connector to CRT yoke assembly.

Video Alignment:

Brightness - use the following procedure to adjust the brightness control on the monitor board.

1. Allow the terminal to warm up for at least five minutes.
2. Increase the screen brightness to maximum level with the ">" key in SETUP mode.
3. Adjust VR402 until the display raster is visible; then back off on the adjustment until the raster disappears.
4. Return the screen brightness to normal viewing intensity with the "<" key in SETUP mode.

Focus - use the following procedure to check and adjust the focus.

1. Type ESC #9 and press the space bar twice.
2. Examine the characters at the four corners and at the center of the screen. The individual dots in the vertical segment of the "E" should be visible in each character.

If the focus is not adjusted satisfactorily, do not perform the following step.

3. Adjust VR403 for the best overall character presentation.

Yoke Rotation - use the following procedure to check and adjust the yoke.

1. Type ESC #8.
2. Verify that the display is aligned to suit personal preference.

Note: If the display is not aligned properly, perform the following steps.

3. Loosen the yoke collar screw and turn the yoke collar until the test pattern appears to be straight both vertically and horizontally.
4. While holding the yoke in place, tighten the yoke collar clamp screw.

Vertical Height - use the following procedure to check and adjust the overall presentation height.

1. Type ESC #9.
2. Verify that the vertical diameter of the circle is approximately 170 mm.

Note: If the vertical diameter is not satisfactory, perform the following step.

3. Adjust VR303 until the vertical diameter is correct.

Horizontal Width - use the following procedure to adjust the overall presentation width.

1. Type ESC #9.
2. Verify that the horizontal diameter of the circle is approximately 170 mm.

Note: If the horizontal diameter is not satisfactory, perform the following step.

3. Adjust L402 until the horizontal diameter is correct.

Centering - use the following procedure to check and adjust the presentation centering.

1. Enter SETUP mode and toggle into 48 line/132 character mode.
2. Adjust VR402 until the display raster is visible.
3. Adjust VR401 until the setup menu is approximately midway between the left and right edges of the raster.
4. Back-off VR402 until the raster disappears.

Vertical Linearity - use the following sequence to check and adjust for uniform presentation height.

1. Type ESC #9.
2. Verify that the vertical radius of the circle is 85 mm to the center and the overall vertical diameter is 170 mm.

Note: If vertical linearity is not satisfactory, perform the following steps.

3. Adjust the vertical linearity using VR302.
4. Check and adjust the vertical height, vertical hold, and centering if required.

Horizontal Linearity - use the following procedure to check and adjust for uniform presentation width.

1. Type ESC #9.
2. Verify the horizontal radius of the circle is 85 mm to the center and overall horizontal diameter is 170 mm.

Note: If the horizontal linearity is not satisfactory, perform the following steps.

3. Adjust the horizontal linearity using L401.
4. Check and adjust the horizontal width, vertical hold, and centering if required.

Vertical Hold - use the following procedure to adjust vertical hold.

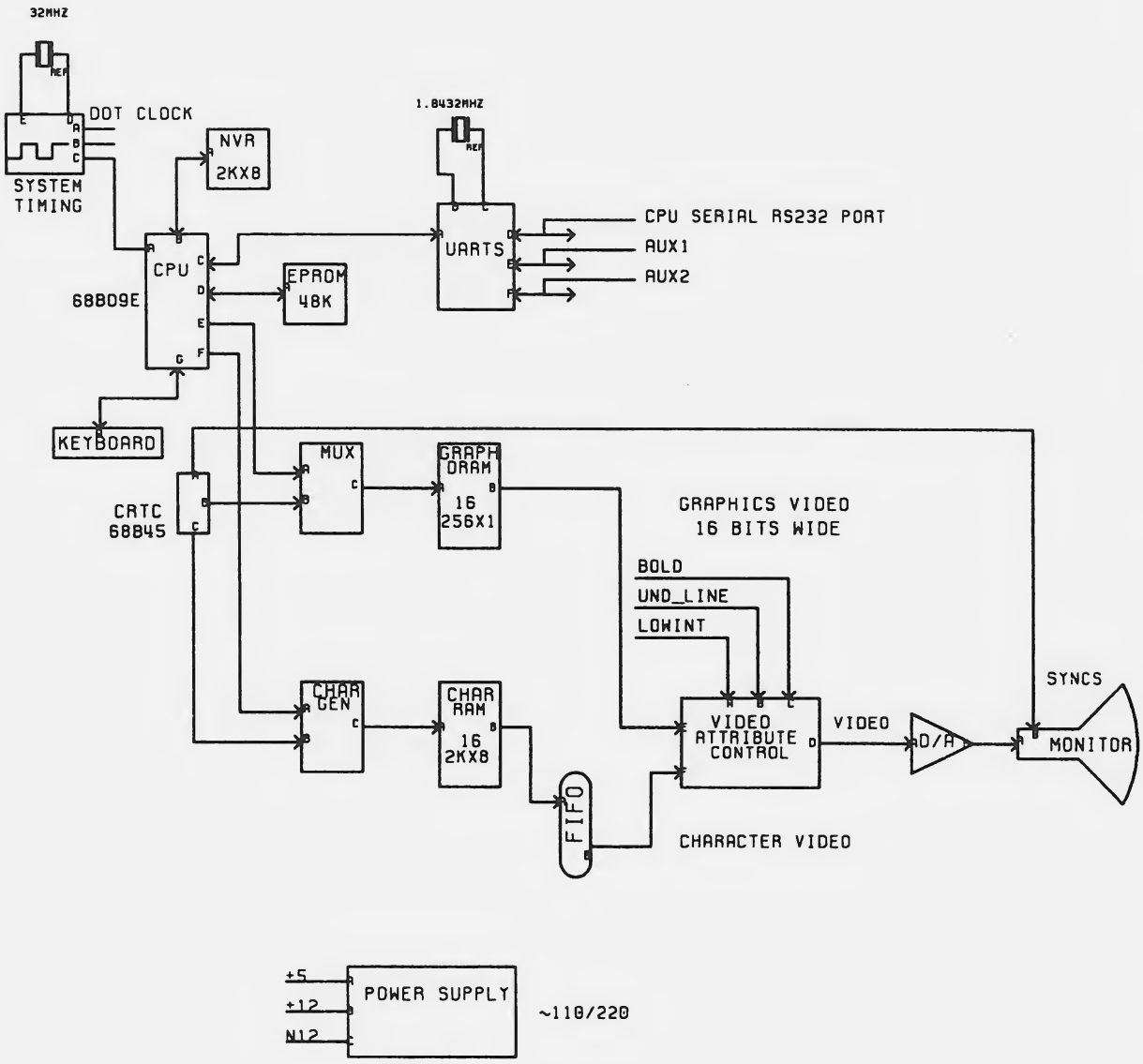
1. Type ESC #9.
2. Adjust VR301 as required until vertical roll ceases.

Appendixes

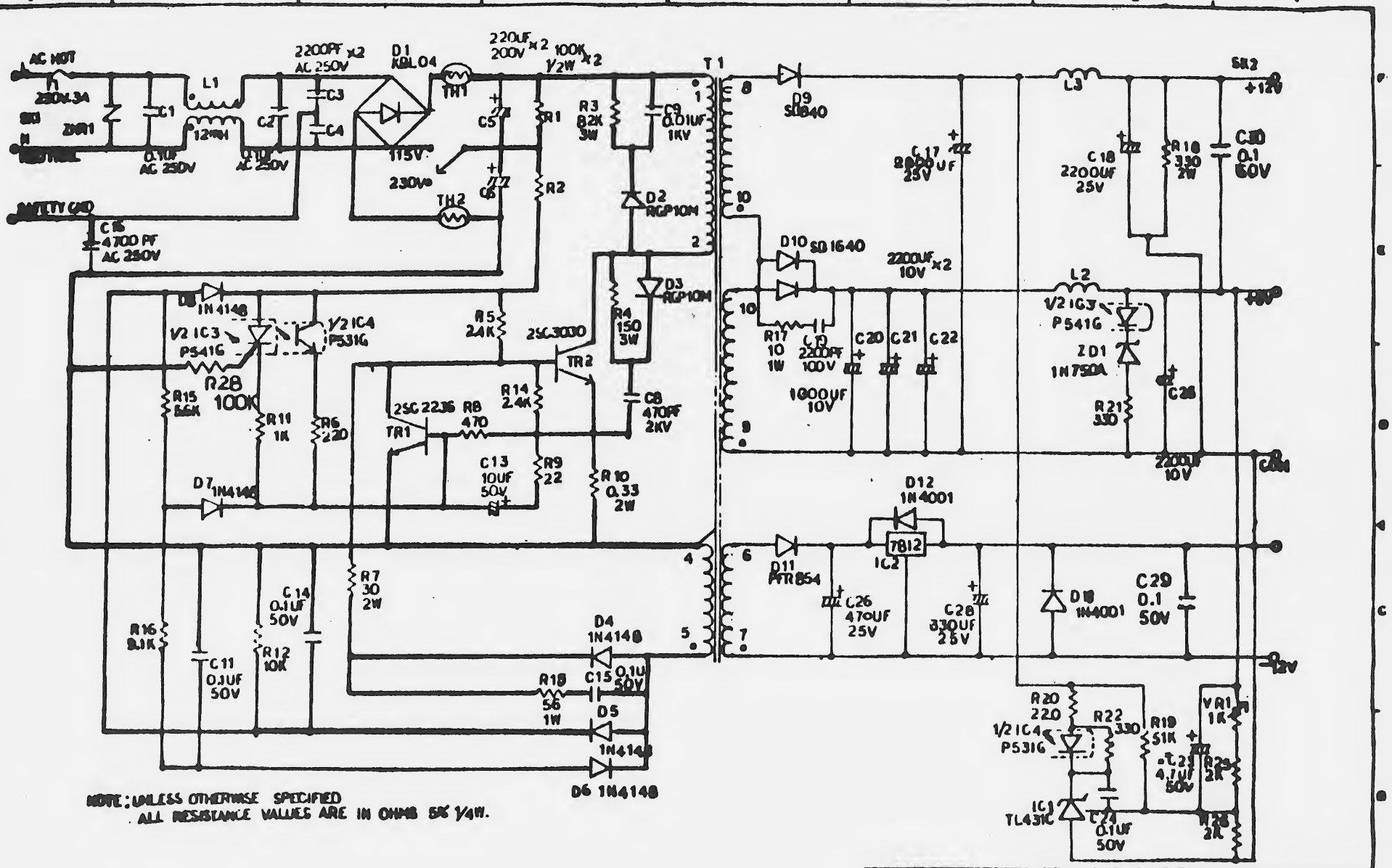
Schematics

This appendix includes diagrams. They appear in the following order:

- System Block Diagram
- Character RAM Timing Diagram
- Graphics RAM Timing Diagram
- Logic Board Schematic
- Video Board Schematic
- Keyboard Schematic
- Power Supply Schematic



Block Diagram

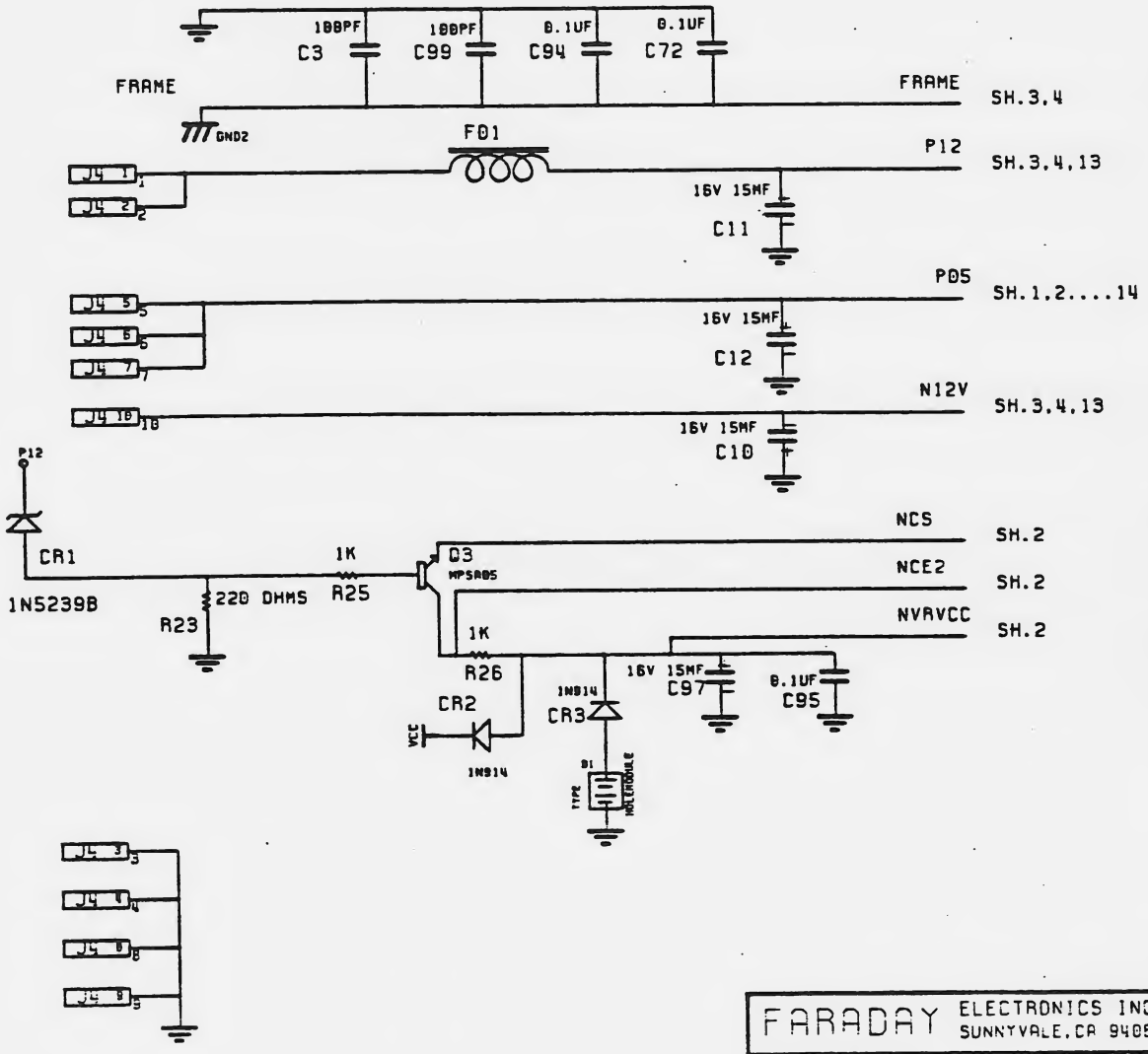


NOTE: UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE VALUES ARE IN OHMS 5% 1/4W.

MATERIAL		FINISH	QTY
REV. NO.	C	DATE	100XL POWER SUPPLY
DRAFTER	Y. J. SEO	85.4.25	FOR A INTERNATIONAL PRODUCTS SERVICE INC.
DRAFTCKR			TITLE
DGN ENGR	S. K. AN		PS70-3
APPROVAL			NEXT ASSY
SCALE	SHEET	OF	DWG NO.

100XL

ASSY. NO. 900-0004-A11



POWER/NVR SWITCH

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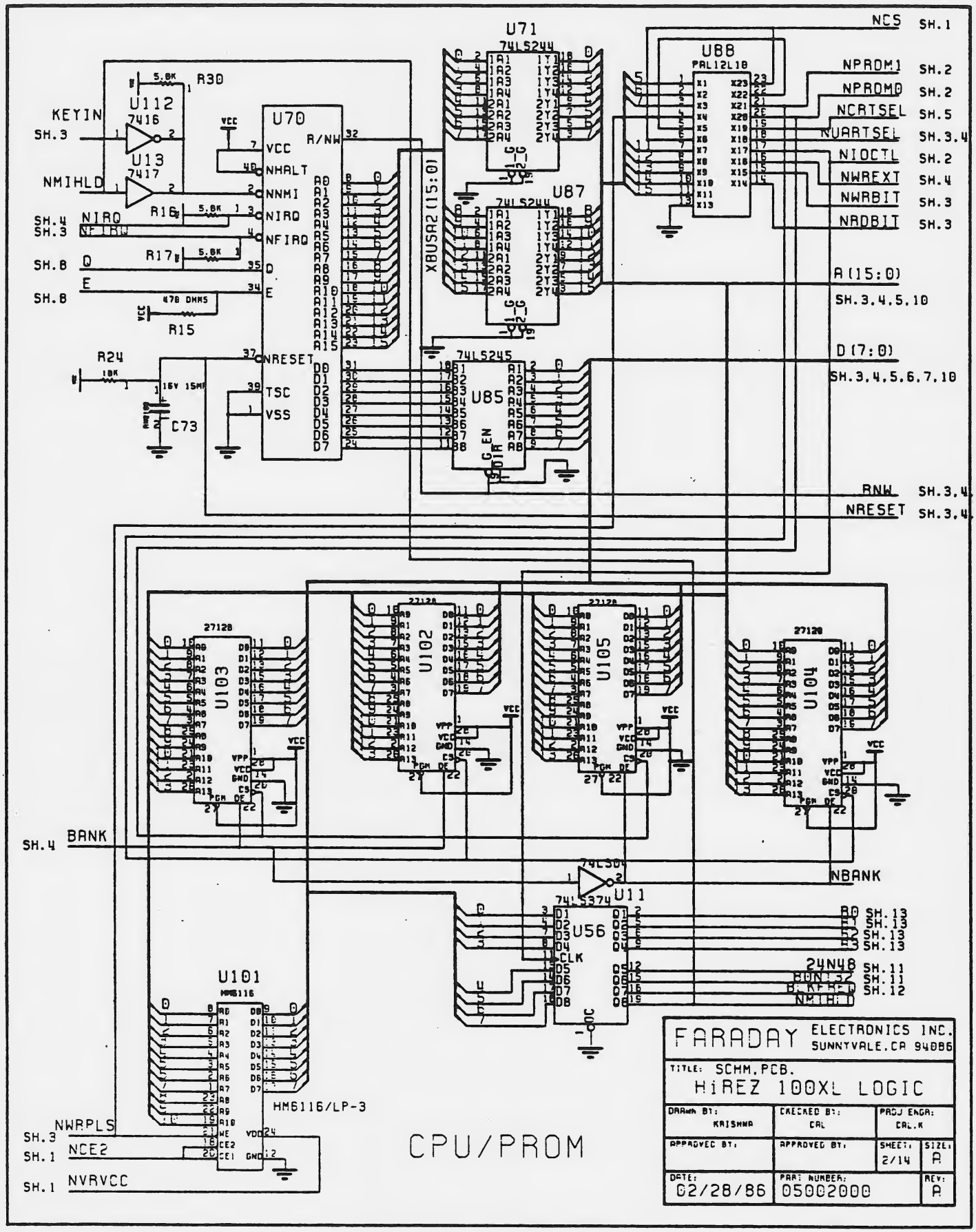
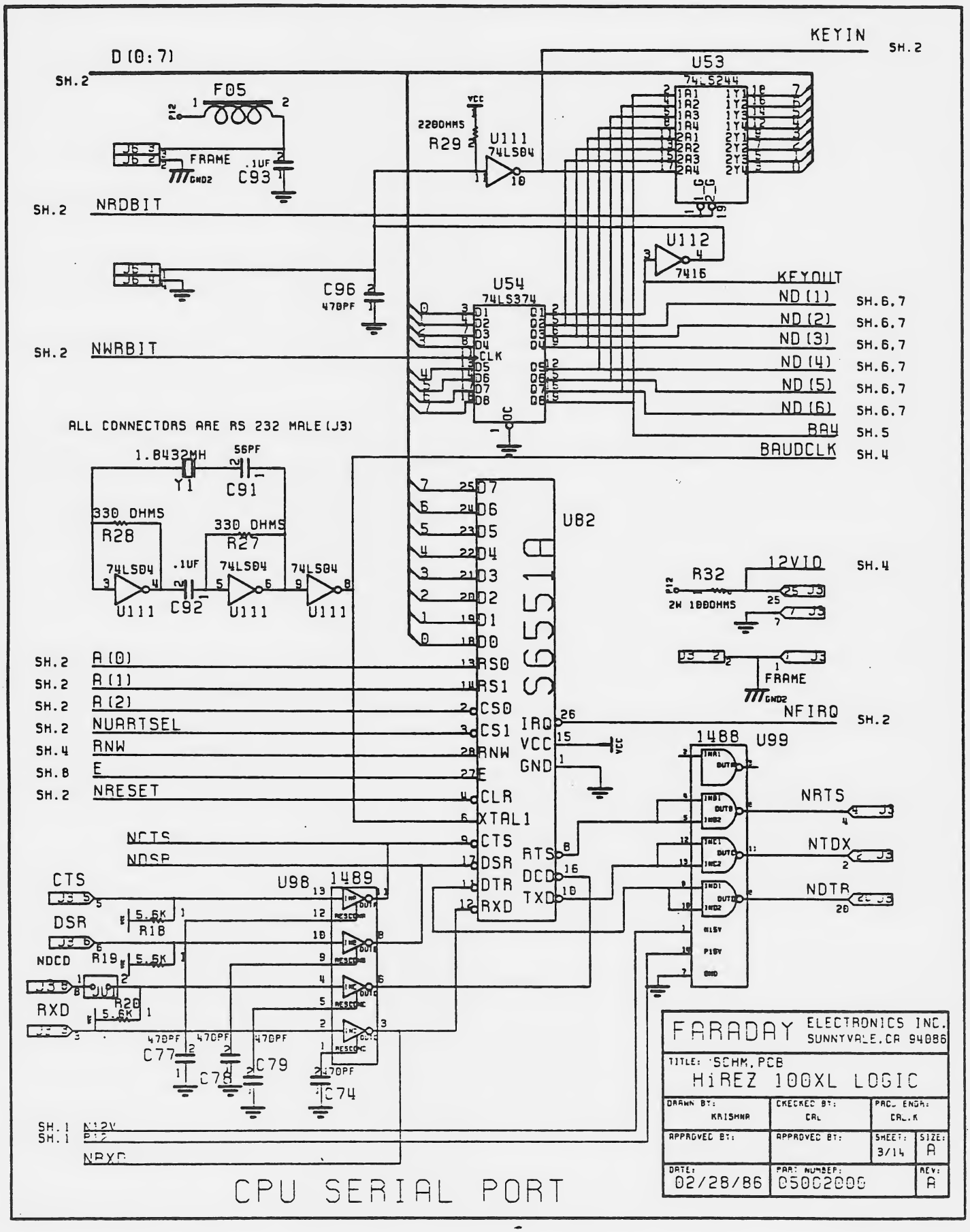
DRAWN BY: KRISHNA	CHECKED BY: CAL	PROJ ENGR: CAL.K	
APPROVED BY:	APPROVED BY:	SHEET: 1/14	SIZE: A
DATE: 02/28/86	PART NUMBER: 05002000		REV: A


U71
74LS244
U88
PAL12L10
NCS SH.1
NPROM1 SH.2
NPROM0 SH.2
NCRTSEL SH.5
NUARTSEL SH.3,4
NIOCTL SH.2
NWREXT SH.4
NWRBIT SH.3
NRDBIT SH.3
U87
74LS244
XBUSA2(15:0)
A(15:0)
SH.3,4,5,10
D(7:0)
SH.3,4,5,6,7,10
U112
7416
U13
7417
KEYIN
SH.3
NMIHLD
SH.4 NIRQ
SH.3 NFIRQ
SH.8 Q
SH.8 E
R30
R16
R17
R15
R24
C73
U70
VCC
NHALT
NNMI
NIRQ
NFIRQ
NRESET
TSC
VSS
R/NW
74LS245
U85
RNW SH.3,4,5
NRESET SH.3,4,5
U103
U102
U105
U104
27128
SH.4 BANK
NBANK
74LS374
U11
U56
CLK
B0 SH.13
B1 SH.13
B2 SH.13
B3 SH.13
24N48 SH.11
BON132 SH.11
BLKFRED SH.12
NMIHLD
U101
HM6116
HM6116/LP-3
NWRPLS
SH.3
SH.1 NCE2
SH.1 NVRVCC
CPU/PROM
FARADAY ELECTRONICS INC.
SUNNYVALE, CA 94086
TITLE: SCHM, PCB.
HiREZ 100XL LOGIC
DRAWN BY: KRISHNA
CHECKED BY: CAL
PROJ ENGR: CAL.K
APPROVED BY:
APPROVED BY:
SHEET: 2/14
SIZE: A
DATE: 02/28/86
PART NUMBER: 05002000
REV: A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D(0:7)
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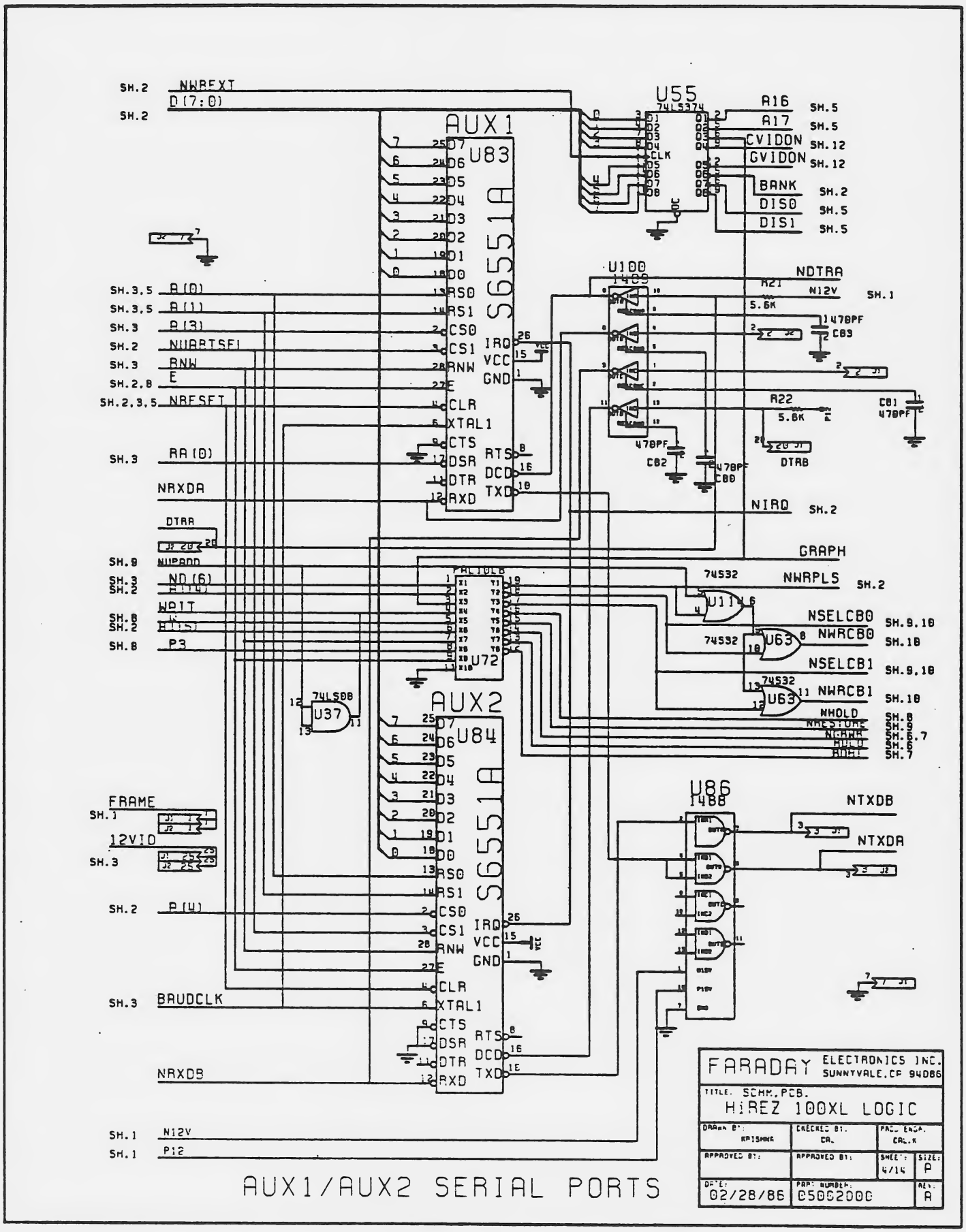
U53
74LS244
F05
FRAME
.1UF
C93
GND2
220OHMS
R29
U111
74LS04
SH.2 NRDBIT
U112
7416
KEYOUT
U54
74LS374
CLK
ND(1) SH.6,7
ND(2) SH.6,7
ND(3) SH.6,7
ND(4) SH.6,7
ND(5) SH.6,7
ND(6) SH.6,7
BAY SH.5
BAUDCLK SH.4
C96
470PF
SH.2 NWRBIT
ALL CONNECTORS ARE RS 232 MALE(J3)
1.8432MH
Y1
56PF
C91
330 OHMS
R28
330 OHMS
R27
74LS04
.1UF
C92
U82
S6551A
R32
12VIO
SH.4
2W 100OHMS
FRAME
NFIRQ
SH.2
SH.2 A(0)
SH.2 A(1)
SH.2 A(2)
SH.2 NUARTSEL
SH.4 RNW
SH.8 E
SH.2 NRESET
NCTS
NDSR
1488
U99
NRTS
NTDX
NDTR
CTS
DSR
NDCD
RXD
U98
1489
5.6K
R18
R19
R20
470PF
C77
C78
C79
C74
SH.1 N12V
SH.1 P12
NRXD
FARADAY ELECTRONICS INC.
SUNNYVALE,CA 94086
TITLE: SCHM,PCB
HiREZ 100XL LOGIC
DRAWN BY: KRISHNA
CHECKED BY: CAL
PROJ ENGR: CAL.K
APPROVED BY:
APPROVED BY:
SHEET: 3/14
SIZE: A
DATE: 02/28/86
PART NUMBER: 05002000
REV: A
CPU SERIAL PORT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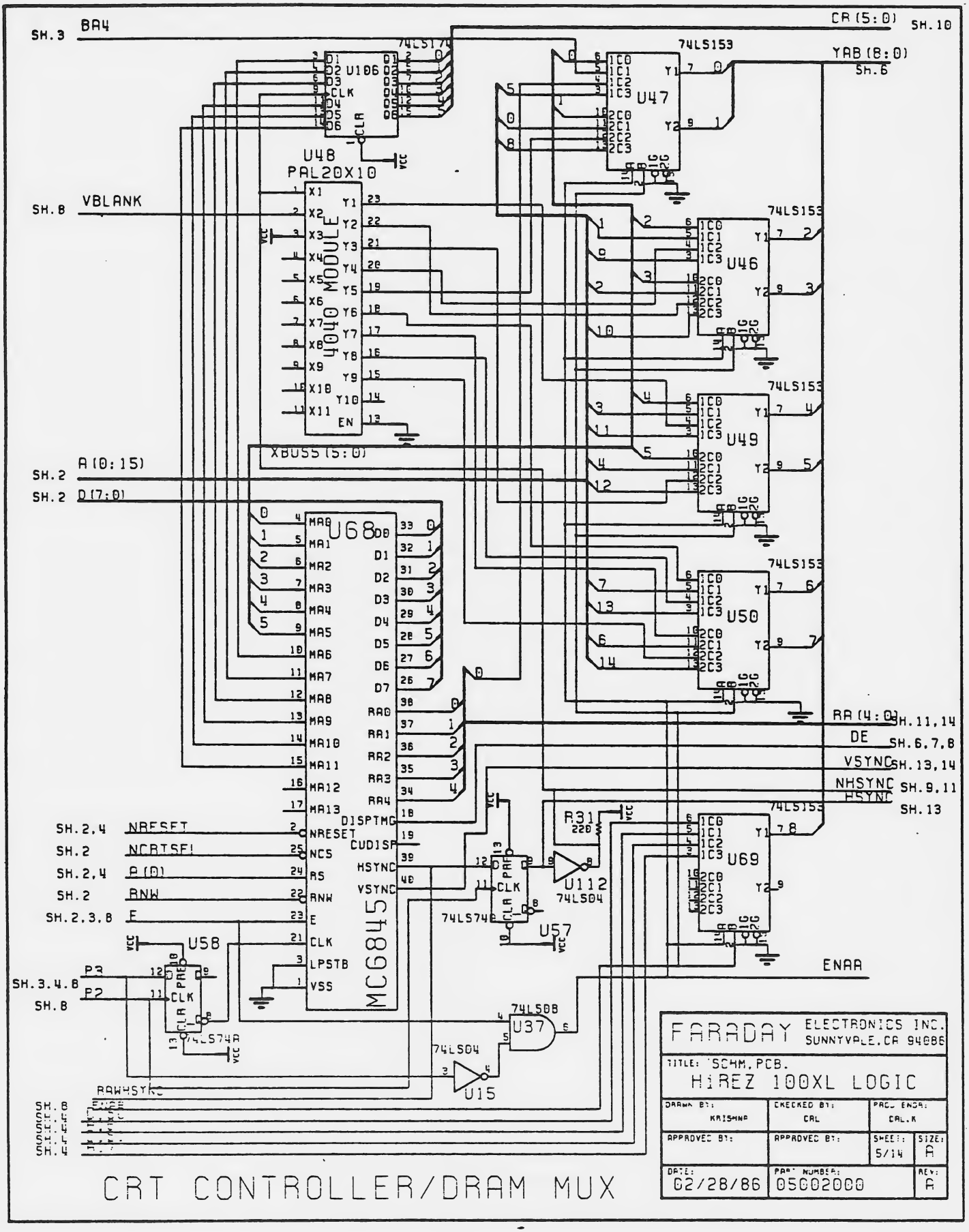
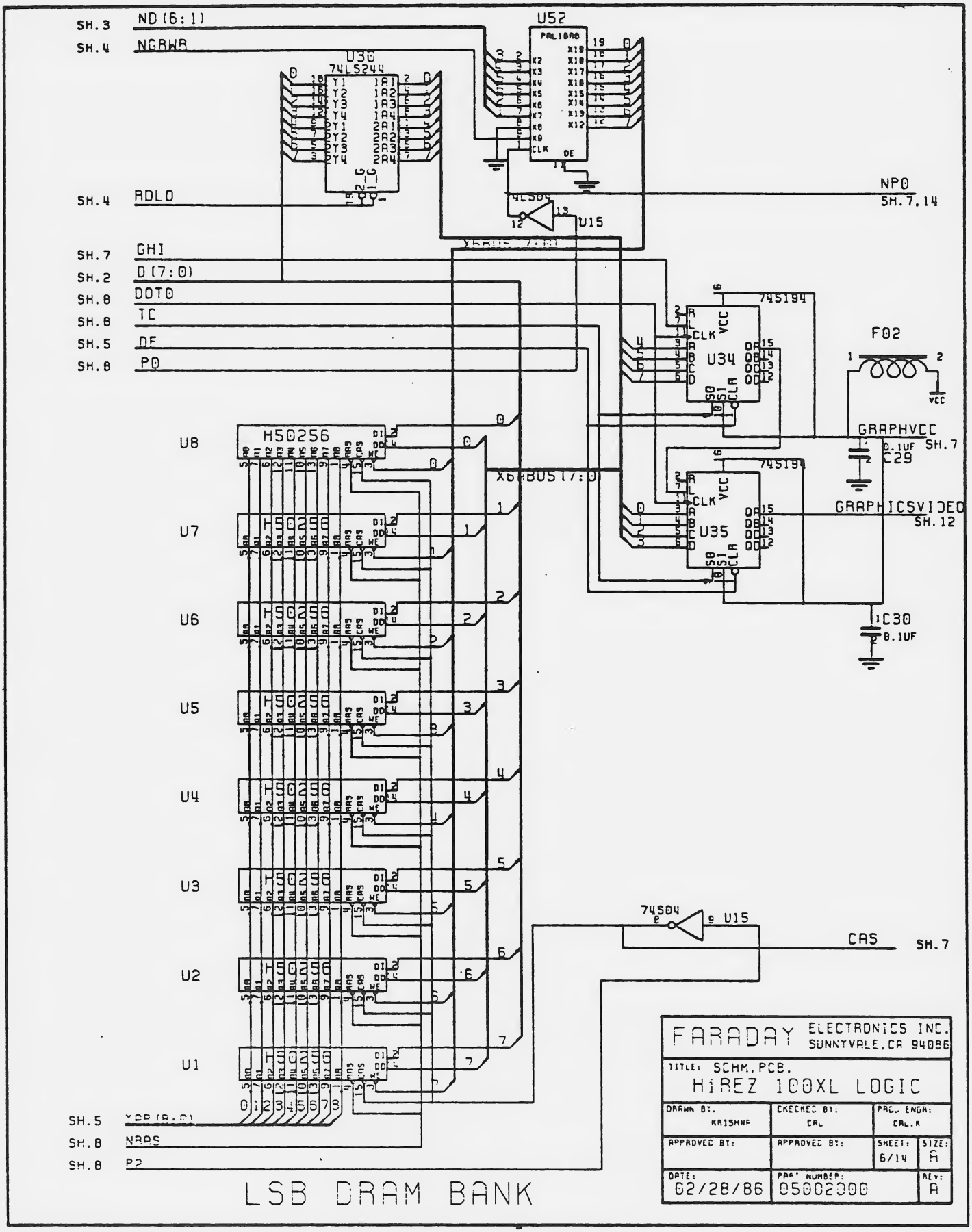
S6551A
AUX2
U84
S6551A
U55
74LS374
U100
74LS00
U72
PAL10L8
U37
74LS08
U86
1488
U63
74S32
U114
74S32
SH.2 NWREXT
D(7:0)
A16 SH.5
A17 SH.5
CVIDON SH.12
GVIDON SH.12
BANK SH.2
DIS0 SH.5
DIS1 SH.5
NDTRA
R21 5.6K
R22 5.6K
N12V SH.1
470PF C83
470PF C81
470PF C82
470PF C80
DTRA
NIRQ SH.2
GRAPH
NWRPLS SH.2
NSELCB0 SH.9,10
NWRCB0 SH.10
NSELCB1 SH.9,10
NWRCB1 SH.10
NHOLD SH.8
NRESTORE SH.9
NCRAM SH.9
AUX1 SH.6,7
AUX2 SH.7
SH.3,5 A(0)
SH.3,5 A(1)
SH.3 A(3)
SH.2 NUARTSEL
SH.3 RNW
SH.2,8 E
SH.2,3,5 NRESET
SH.3 RA(0)
NRXDA
DTRA
SH.9 NUPADD
SH.3 ND(6)
SH.2 A(14)
WAIT
SH.8
SH.2 A(15)
SH.8 P3
FRAME SH.1
12VID SH.3
SH.2 P(4)
SH.3 BAUDCLK
NRXDB
NTXDB
NTXDA
SH.1 N12V
SH.1 P12
FARADAY ELECTRONICS INC.
SUNNYVALE,CA 94086
TITLE: SCHM.PCB.
HIREZ 100XL LOGIC
DRAWN BY: KRISHNA
CHECKED BY: CR.
PROJ ENGR: CRL.K
APPROVED BY:
APPROVED BY:
SHEET: 4/16
SIZE: D
DATE: 02/28/86
PART NUMBER: 05002000
REV: A
AUX1/AUX2 SERIAL PORTS



SH.3 BA4
CR (5:0) SH.10
YAB (8:0) SH.6
74LS174
U106
74LS153
U47
U48
PAL20X10
4040 MODULE
SH.8 VBLANK
U46
U49
U50
XBUSS (5:0)
SH.2 A (0:15)
SH.2 D (7:0)
U68
MC6845
RA (4:0) SH.11,14
DE SH.6,7,8
VSYNC SH.13,14
NHSYNC SH.9,11
HSYNC SH.13
SH.2,4 NRESET
SH.2 NCRTSEL
SH.2,4 A (0)
SH.2 RNW
SH.2,3,8 E
U69
R31 220
U112 74LS04
74LS74A
U57
U58
SH.3,4,8 P3
SH.8 P2
74LS74A
ENAA
74LS08
U37
74LS04
U15
RAWHSYNC
SH.8
SH.4
SH.4
SH.4
SH.4
FARADAY ELECTRONICS INC.
SUNNYVALE, CA 94086
TITLE: SCHM, PCB.
HiREZ 100XL LOGIC
DRAWN BY: KRISHNA
CHECKED BY: CAL
PROJ ENGR: CAL.K
APPROVED BY:
APPROVED BY:
SHEET: 5/14
SIZE: A
DATE: 02/28/86
PART NUMBER: 05002000
REV: A
CRT CONTROLLER/DRAM MUX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SH.4 NGRWR
U30
74LS244
U52
SH.4 RDLO
NP0
SH.7.14
U15
SH.7 GHI
SH.2 D(7:0)
SH.8 DOTO
SH.8 TC
SH.5 DF
SH.8 PO
74S194
U34
F02
VCC
GRAPHVCC
0.1UF
C29
SH.7
U8
H50256
U35
GRAPHICSVIDEO
SH.12
X64BUS(7:0)
U7
U6
U5
U4
U3
U2
U1
C30
0.1UF
74S04
U15
CAS
SH.7
SH.5 YBR(8:0)
SH.8 NRAS
SH.8 P2
LSB DRAM BANK
FARADAY ELECTRONICS INC.
SUNNYVALE,CA 94086
TITLE: SCHM,PCB.
HiREZ 100XL LOGIC
DRAWN BY:
CHECKED BY:
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APPROVED BY:
SHEET: 6/14
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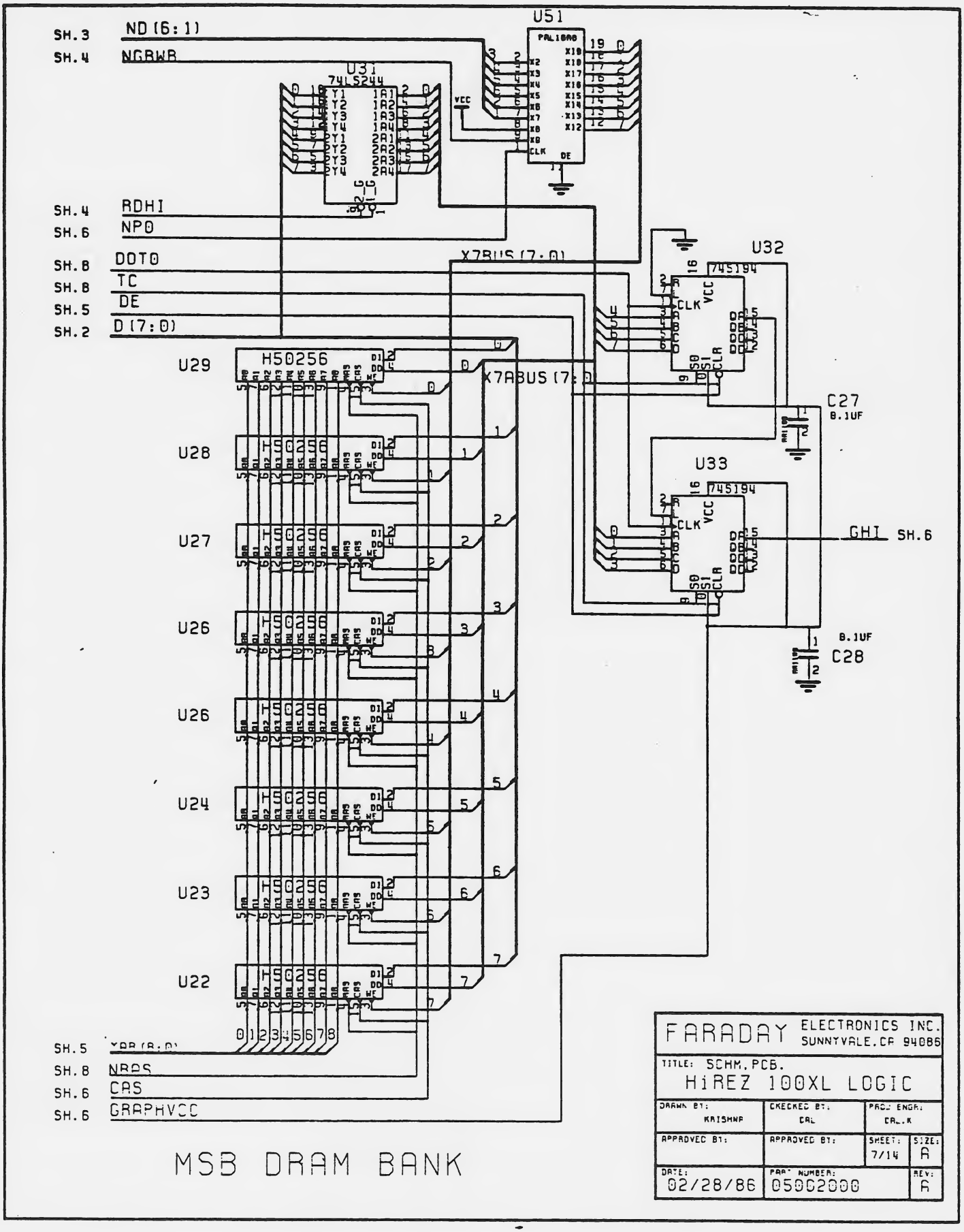
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SH.4 NGBWB
U51
PAL16R8
U31
74LS244
SH.4 RDHI
SH.6 NPD
SH.8 DOTD
SH.8 TC
SH.5 DE
SH.2 D(7:0)
X7BUS(7:0)
U32
74S194
C27
0.1UF
U33
74S194
GHI SH.6
0.1UF
C28
U29
H50256
U28
U27
U26
U26
U24
U23
U22
0 1 2 3 4 5 6 7 8
SH.5
SH.8 NRAS
SH.6 CAS
SH.6 GRAPHVCC
MSB DRAM BANK
FARADAY ELECTRONICS INC.
SUNNYVALE,CA 94086
TITLE: SCHM,PCB.
HiREZ 100XL LOGIC
DRAWN BY: KRISHNA
CHECKED BY: CAL
PROJ ENGR: CAL.K
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SHEET: 7/14
SIZE: A
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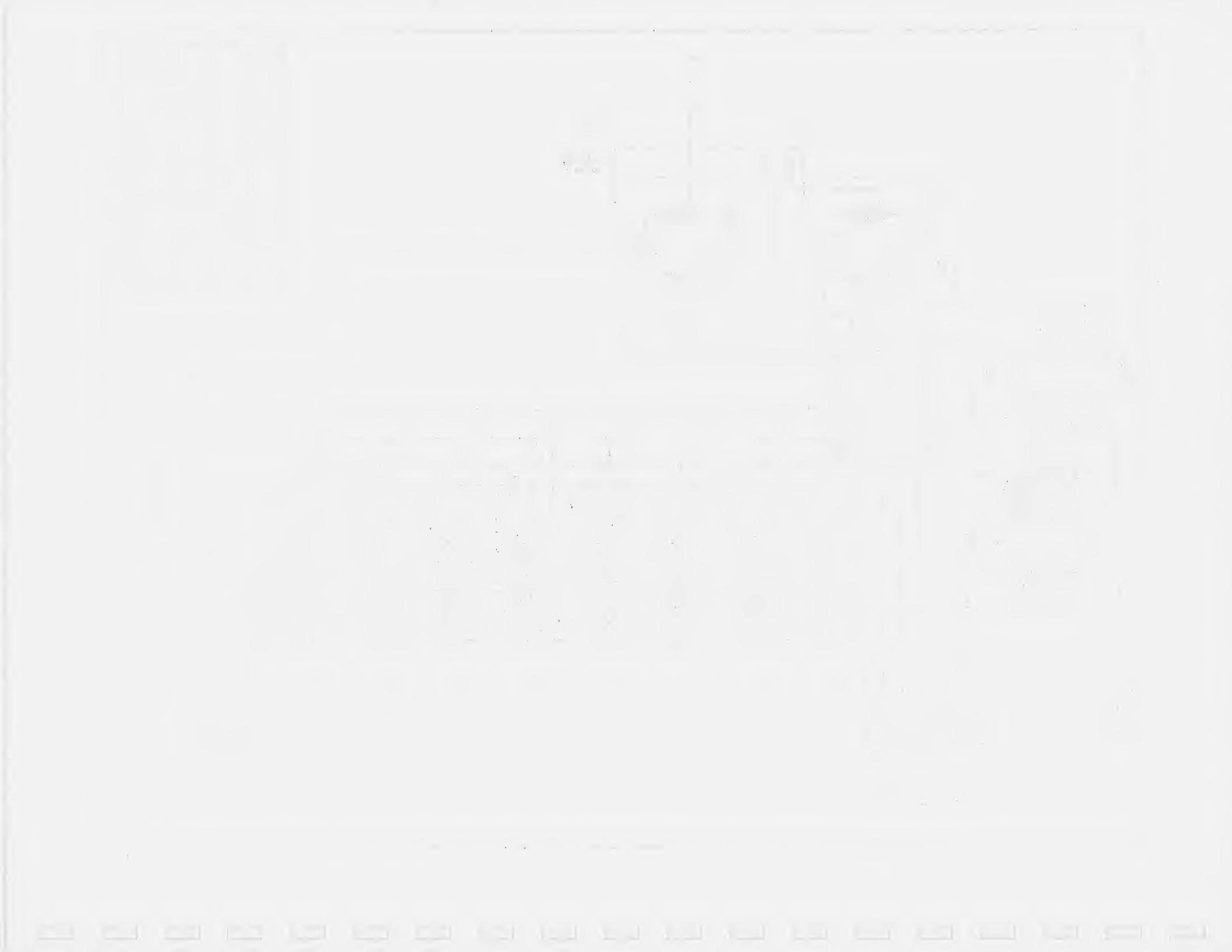
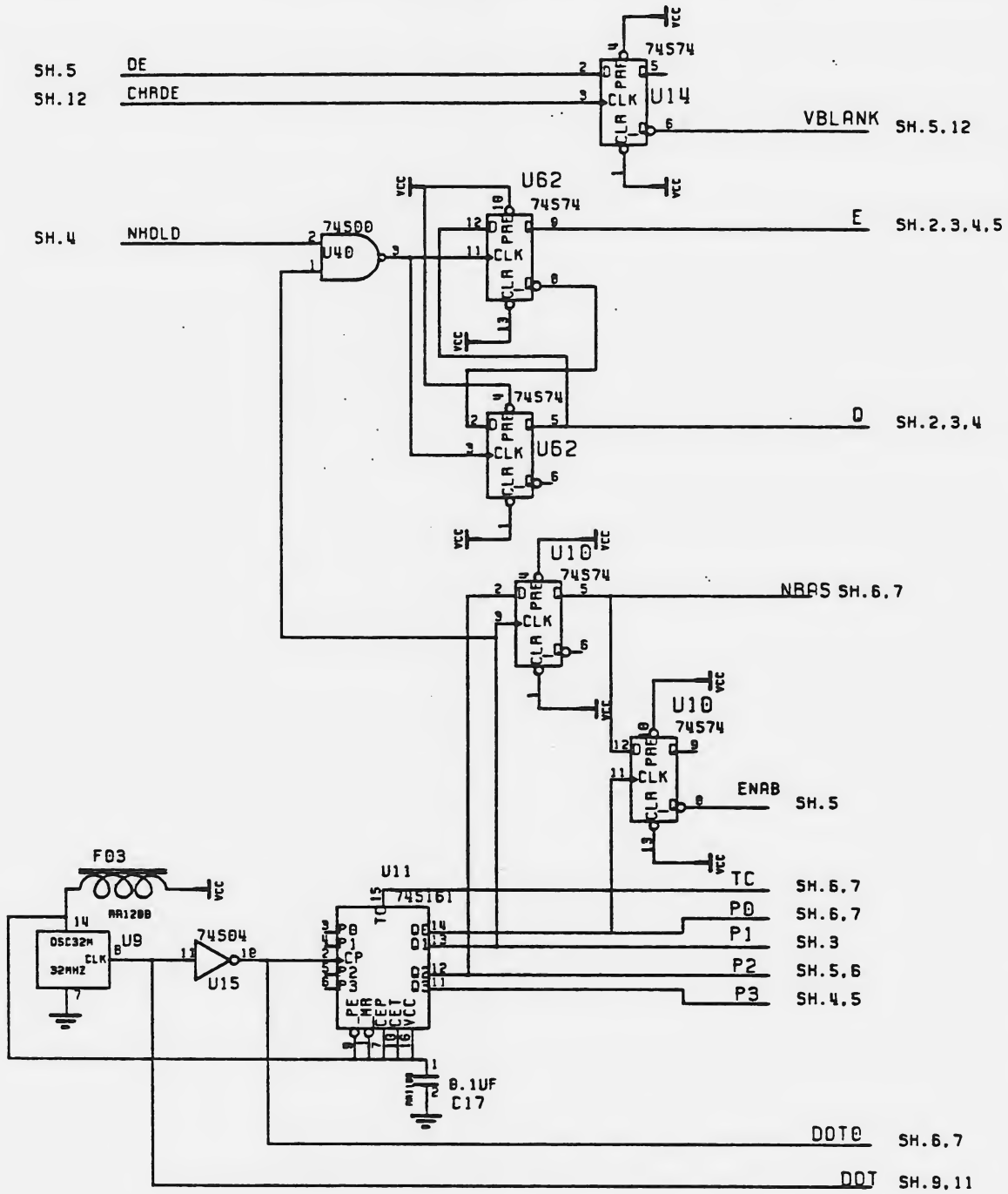
REV: A





SYSTEM CLOCKS

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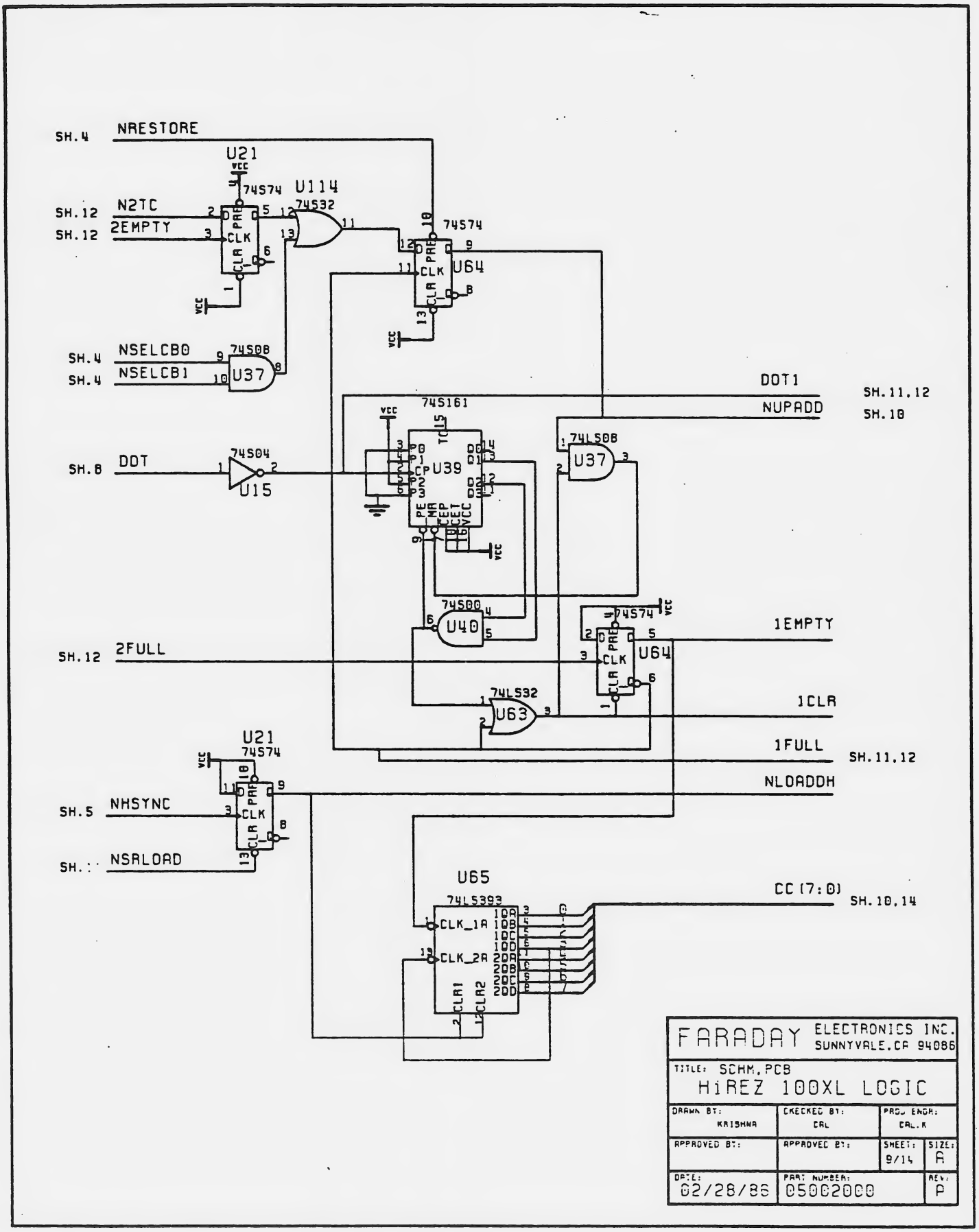
APPROVED BY:	APPROVED BY:	SHEET: 8/14	SIZE: A
DATE: 02/28/86	PART NUMBER: 05002000		REV: A


SH.4 NRESTORE
U21
74S74
U114
74S32
SH.12 N2TC
SH.12 2EMPTY
74S74
U64
SH.4 NSELCB0
SH.4 NSELCB1
74S08
U37
DOT1
NUPADD
SH.11.12
SH.10
74S161
U39
74LS08
U37
SH.8 DOT
74S04
U15
74S00
U40
74S74
U64
1EMPTY
SH.12 2FULL
74LS32
U63
1CLR
1FULL
SH.11.12
NLOADDH
U21
74S74
SH.5 NHSYNC
SH.: NSRLOAD
U65
74LS393
CC(7:0)
SH.10,14
FARADAY ELECTRONICS INC.
SUNNYVALE,CA 94086
TITLE: SCHM,PCB
HiREZ 100XL LOGIC
DRAWN BY: KRISHNA
CHECKED BY: CAL
PROJ ENGR: CAL.K
APPROVED BY:
APPROVED BY:
SHEET: 9/14
SIZE: A
DATE: 02/28/86
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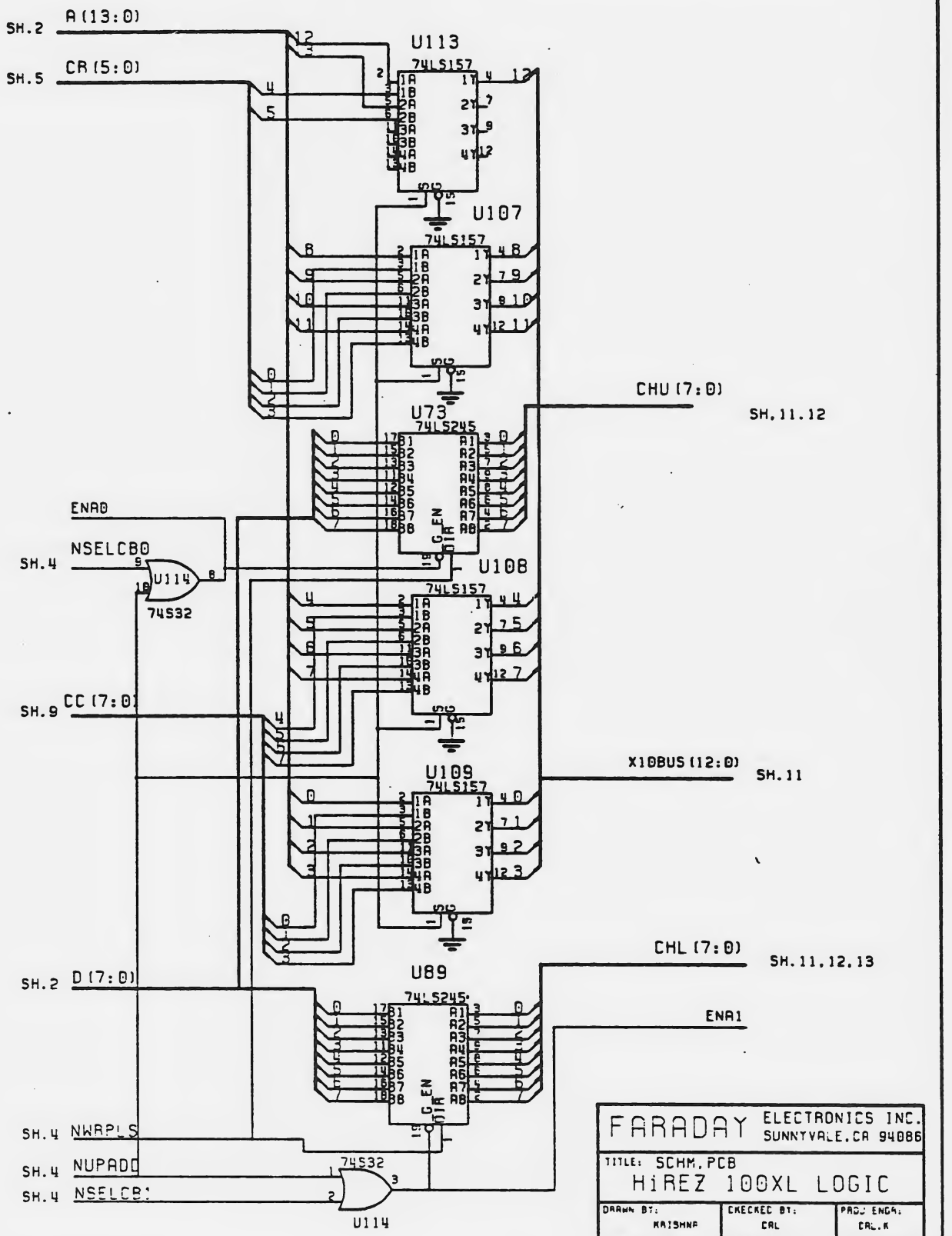
REV: P


SH.2 A(13:0)
SH.5 CR(5:0)
U113
74LS157
U107
74LS157
U73
74LS245
CHU(7:0)
SH.11.12
ENA0
SH.4 NSELCB0
U114
74S32
U108
74LS157
SH.9 CC(7:0)
X10BUS(12:0)
SH.11
U109
74LS157
CHL(7:0)
SH.11,12,13
SH.2 D(7:0)
U89
74LS245
ENA1
SH.4 NWRPLS
SH.4 NUPADD
SH.4 NSELCB1
74S32
U114
CHARACTER MUX
FARADAY ELECTRONICS INC.
SUNNYVALE,CA 94086
TITLE: SCHM,PCB
HiREZ 100XL LOGIC
DRAWN BY: MAISHNR
CHECKED BY: CRL
PROJ ENGR: CRL.K
APPROVED BY:
APPROVED BY:
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DATE: 02/28/86
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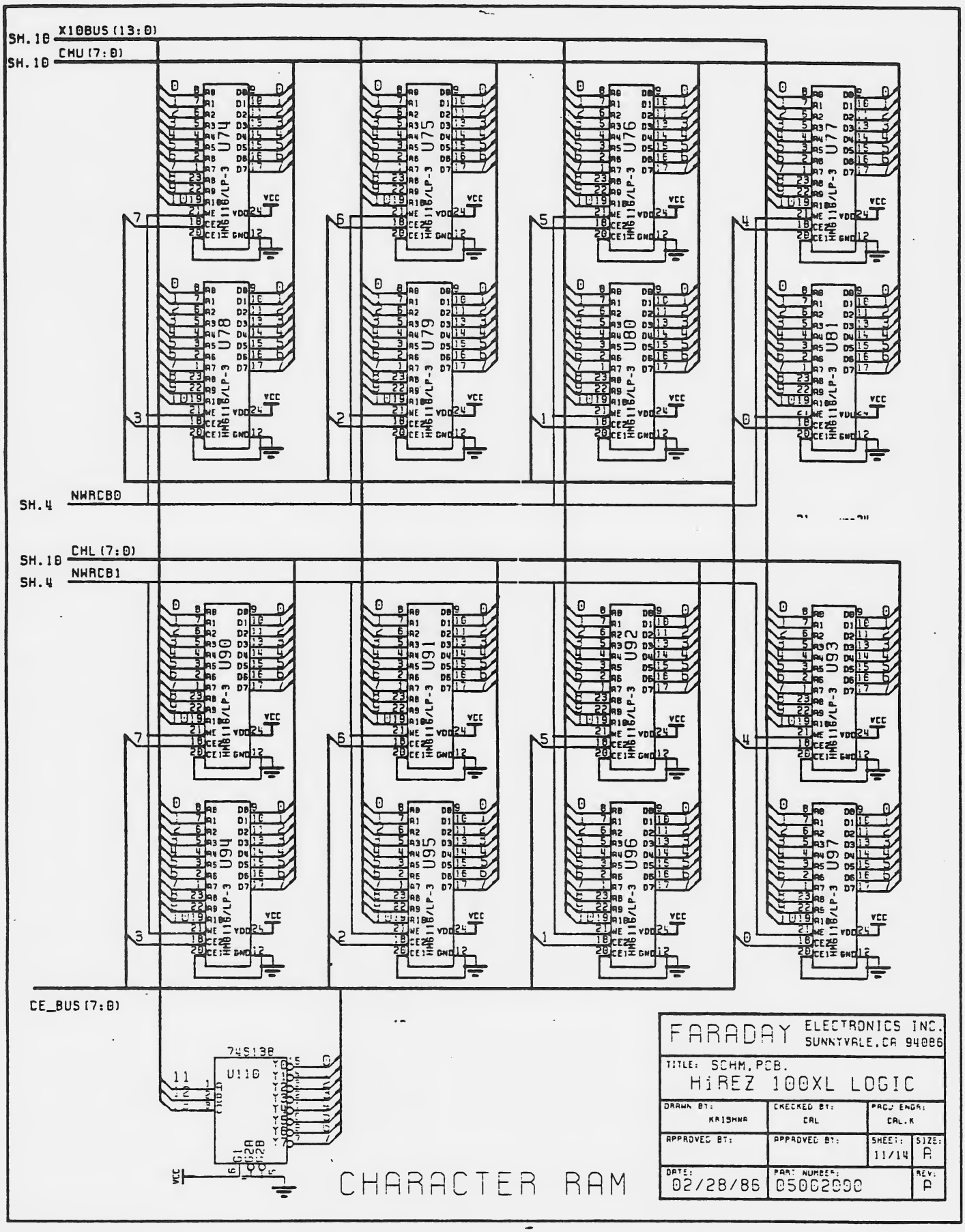
REV: A



FARADAY ELECTRONICS INC. SUNNYVALE,CA 94086		
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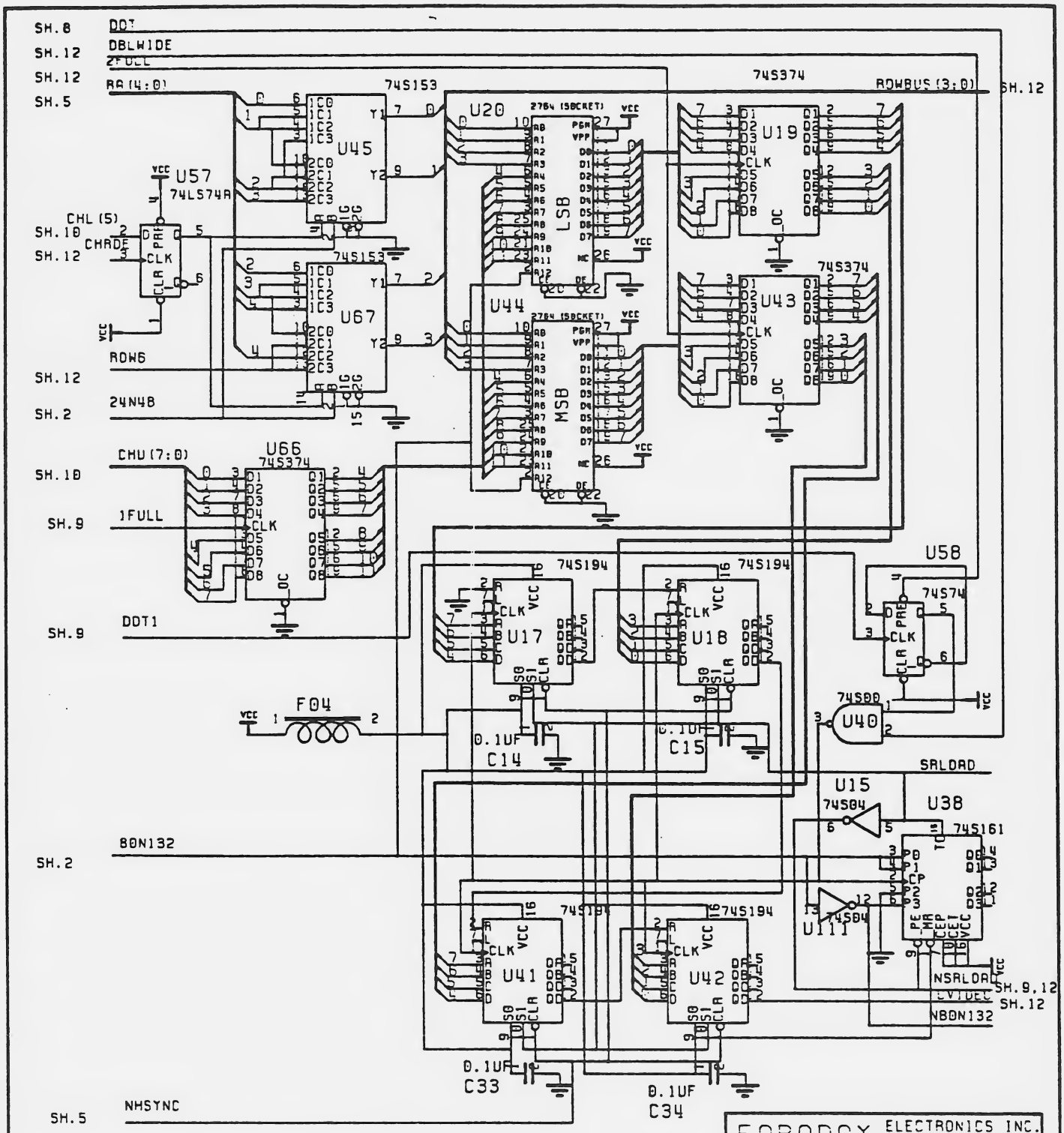

FARADAY ELECTRONICS INC. SUNNYVALE,CA 94086		
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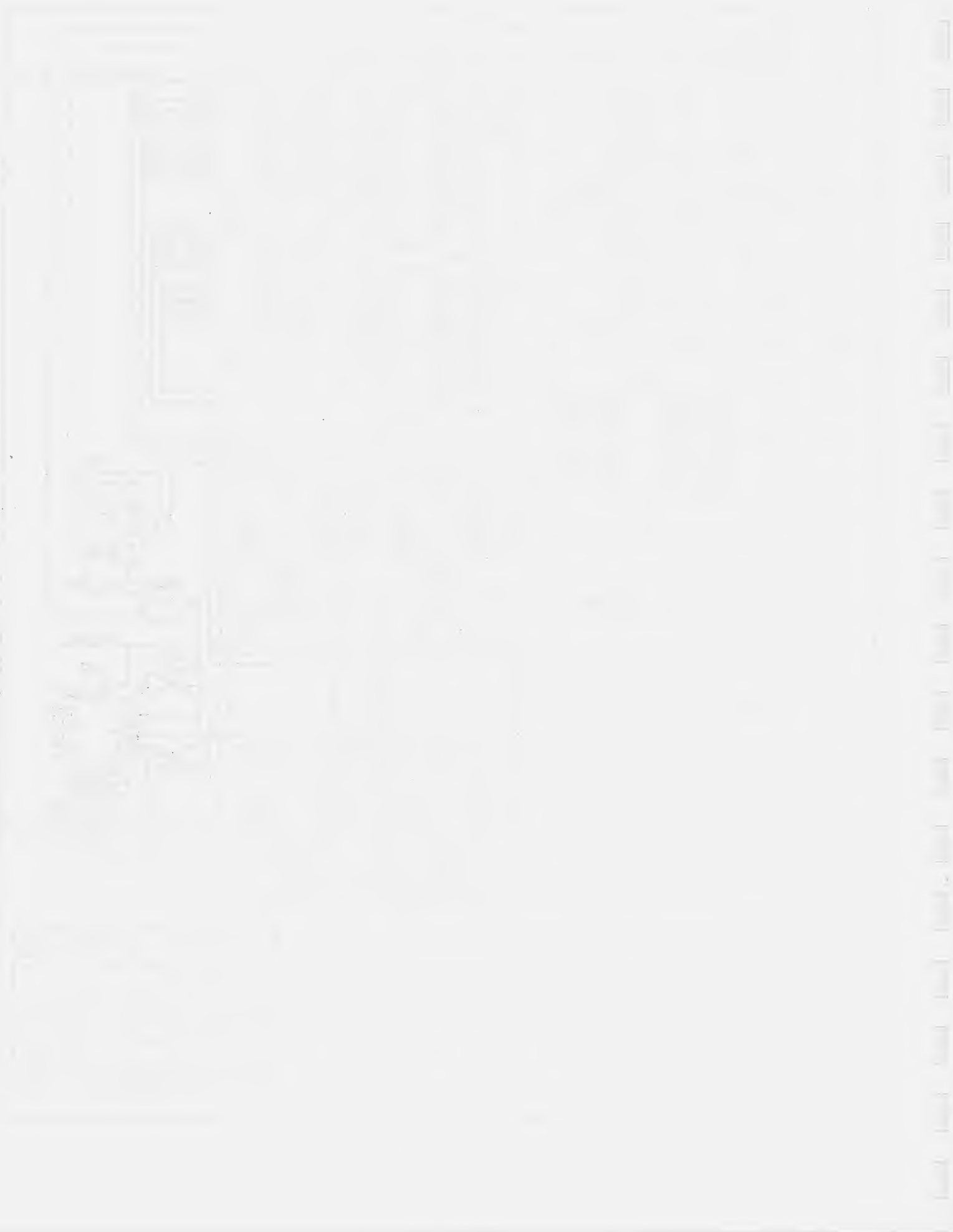
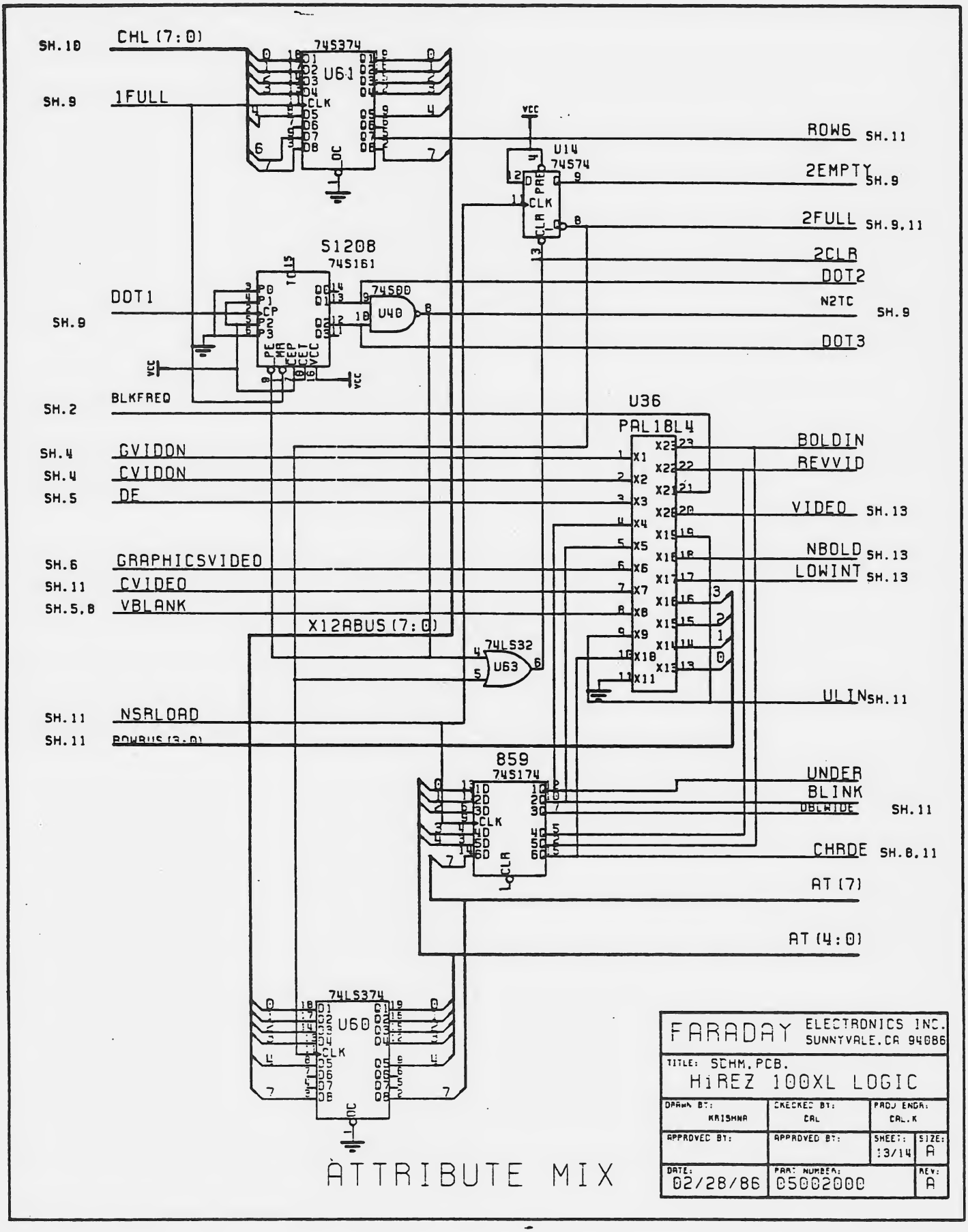
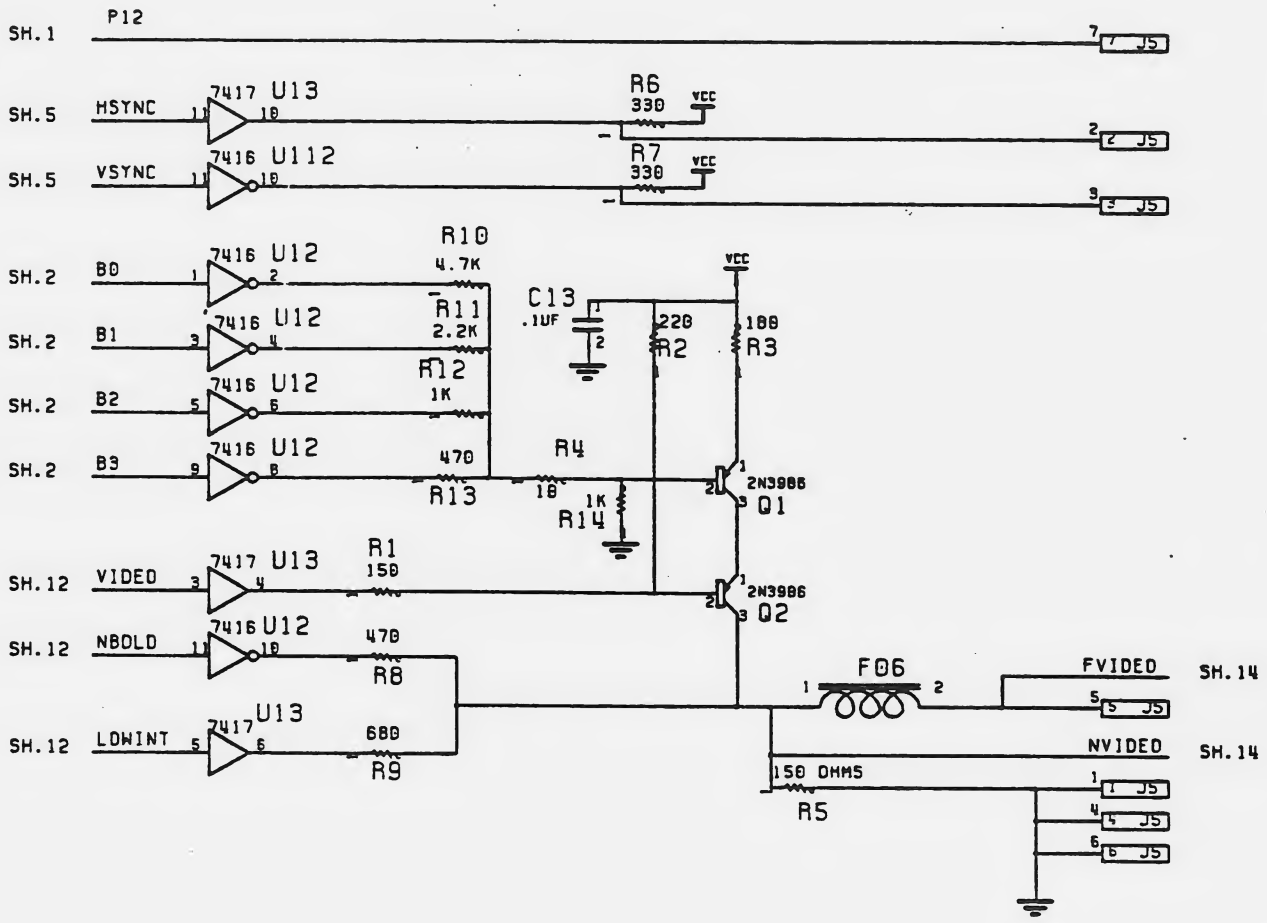
APPROVED BY:	APPROVED BY:	SHEET: 12/14 SIZE: A
DATE: 02/06/86	PART NUMBER: 05002000	REV: A

CHARACTER GENERATOR




SH.10
CHL (7:0)
74S374
U61
SH.9
1FULL
CLK
OC
VCC
U14
74S74
PRE
CLR
ROW6 SH.11
2EMPTY SH.9
2FULL SH.9,11
2CLR
DOT2
N2TC SH.9
DOT3
S1208
74S161
DOT1
SH.9
74S00
U40
BLKFRED
SH.2
U36
PAL18L4
SH.4 GVIDON
SH.4 CVIDON
SH.5 DF
BOLDIN
REVVID
VIDEO SH.13
NBOLD SH.13
LOWINT SH.13
SH.6 GRAPHICSVIDEO
SH.11 CVIDEO
SH.5,8 VBLANK
X12ABUS (7:0)
74LS32
U63
ULIN SH.11
SH.11 NSRLOAD
SH.11 ROWBUS (3:0)
859
74S174
UNDER
BLINK
DBLWIDE SH.11
CHRDE SH.8,11
AT (7)
AT (4:0)
74LS374
U60
ATTRIBUTE MIX
FARADAY ELECTRONICS INC.
SUNNYVALE,CA 94086
TITLE: SCHM,PCB.
HiREZ 100XL LOGIC
DRAWN BY: KRISHNA
CHECKED BY: CAL
PROJ ENGR: CAL.K
APPROVED BY:
APPROVED BY:
SHEET: 13/14
SIZE: A
DATE: 02/28/86
PART NUMBER: 05002000
REV: A



VIDEO

FARADAY ELECTRONICS INC. SUNNYVALE, CA 94086			
TITLE: SCHM.PCB HiREZ 100XL LOGIC			
DRAWN BY: KRISHNA	CHECKED BY: CAL	PROJ. ENGR: CAL.K	
APPROVED BY:	APPROVED BY:	SHEET: 14/14	SIZE: A
DATE: 02/28/86	PART NUMBER: 05002000		REV: A

DWG. NO.	SH	REV.

REVISIONS

ZONE	LTR	DESCRIPTION	CHECK	DATE	APPROVED
	A	INITIAL RELEASE	J. SINN	2/20/86	

PWB 1103

PWB 1203

VIDEO 8
VIDEO VERTICAL GROUND 10
+12 V 7
NC 5
VERTICAL SYNC 9
REMOTE BRIGHTNESS CONTROL CUSTOMERS 2 4 3
HORIZONTAL SYNC 6
HORIZONTAL GROUND 7

C201 470
R201 75
VR201 1KB INT. CONT
.22uF
L301
R301 1 1/2W
D302 IN4002
C304 100/16
C308 0.001
VR303 300KB V SIZE
R315 180K
IC301 TDA1170S
2 5 3 7 4 9 6 12 TABS 10 11 8
C313 2200/16
R313 68K
C309 39P
R312 1.8K
C310 1000P
R314 3.3 1/2W RN
C302 0.01
D301 IN00
R303 2.2K
R302 6.8K
R304 18K
VR301 100KB V HOL - D
R305 120K
C303 0.15
R306 820K
C305 0.1
C306 0.1
R307 47K
R308 56K
VR302 300KB V LIN
C307 0.01
R309 4.7K
R311 5.6K
R310 1 1/2W RN
C311 100/16
C312 0.1
C301 100/16

BLUE K K
GND KG KG GND
PNK H H

R205 1K
TR202 BF258
TR201 2N2222A
R206 1K
C203 47/25
R208 1K
D201
C202 0.1
C204 330P
R207 47K
R203 68
BZX83C6V2

R901 100 1/2W
L201 4.7UH
SG901
SG902
ARC GND
R902 1K 1/2W RC
R904 4.7K 1/2W RC
R903 4.7K 1/2W RC

V901
CRT
R5121P39 - SDHT
OR
R14AP39 - DH

GND H G1 G2 G4

C417 680P
R413 1K 1/2W RN
D1 YEL
D2 BRN
D3 BLUE
D4 VIOLET
L302
L404
TMD - 2738

P YEL 61 ORN G2 RED G4 PNK
R209 820 2W RN INT BRIGHT
VR402 100KB

VID. CNTR
C401 2200/16
R405 100
VR401 20KB
R410 27K
R420 0.47 1W
R403 5.6K
R404 5.6K
D401 1S1555
C402 470P
D401 1S1555
IC401 NC1455 NE555
R406 10K
R407 5.6K
C404 0.1
C406 0.001
D402 1S1555
C405 1000P
C407 700P
R409 15K
R408 560
IC402 NC1455 NE555
C408 0.01
IRF740 D G S
C410 0.1
R402 10K
TR401 KTC1815
R401 6.8K

T401 TMF-2224
D405 PFR854
C424 100/16
C416 100/50
L402 HW 745 H SIZE
L401 H-4631 H LIN
C413 822/630
C414 1.3/250
D406 R6P10J PLR817
C415 332/630
R415 1 1/2W RN
D410 R6P10J PLR817
D407 R6P10J IN4002
R6P10J PLR817
C418 22/160
C419 47/100
C420 0.047/630
C421 0.01/630
C422 33/100
C423 0.022
R416 22K
D409 R6P10J IN4002
R417 47K
R418 100K
VR403 2MB FOCUS
R419 220K

BLACK H-GND

SI METRIC	ITEM NO	REQD	PART NUMBER	DESCRIPTION	MATL SPEC	REF DES	CODE IDENT
				LIST OF MATERIALS			

THIRD ANGLE PROJECTION

FIRST USED MODEL

NEXT ASSEMBLY

DO NOT SCALE DRAWING

UNLESS OTHERSIES NOTED:
1. ALL DIMENSIONS ARE IN MILLIMETRES.
2. BREAK ALL SHARP EDGES.
3. DIMENSIONS APPLY AFTER FINISHING, HEAT TREATING AND PLATING.

TOLERANCES:

ANGULAR:	±0.5°	
OVER:—	TO: 25	= ±0.2 (.008)
OVER: 25	TO: 100	= ±0.3 (.012)
OVER: 100	TO: 200	= ±0.5 (.020)
OVER: 200	TO: 300	= ±0.7 (.028)
OVER: 300	TO: 500	= ±0.9 (.035)
OVER: 500		= ±1 (.039)

DR	J. SINN	
CHK		
APP		
APP		
APP		
MATL		
FINISH		

FARADAY

TITLE: MONITOR CIRCUIT HIREZ - 100XL

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D		01009000	A

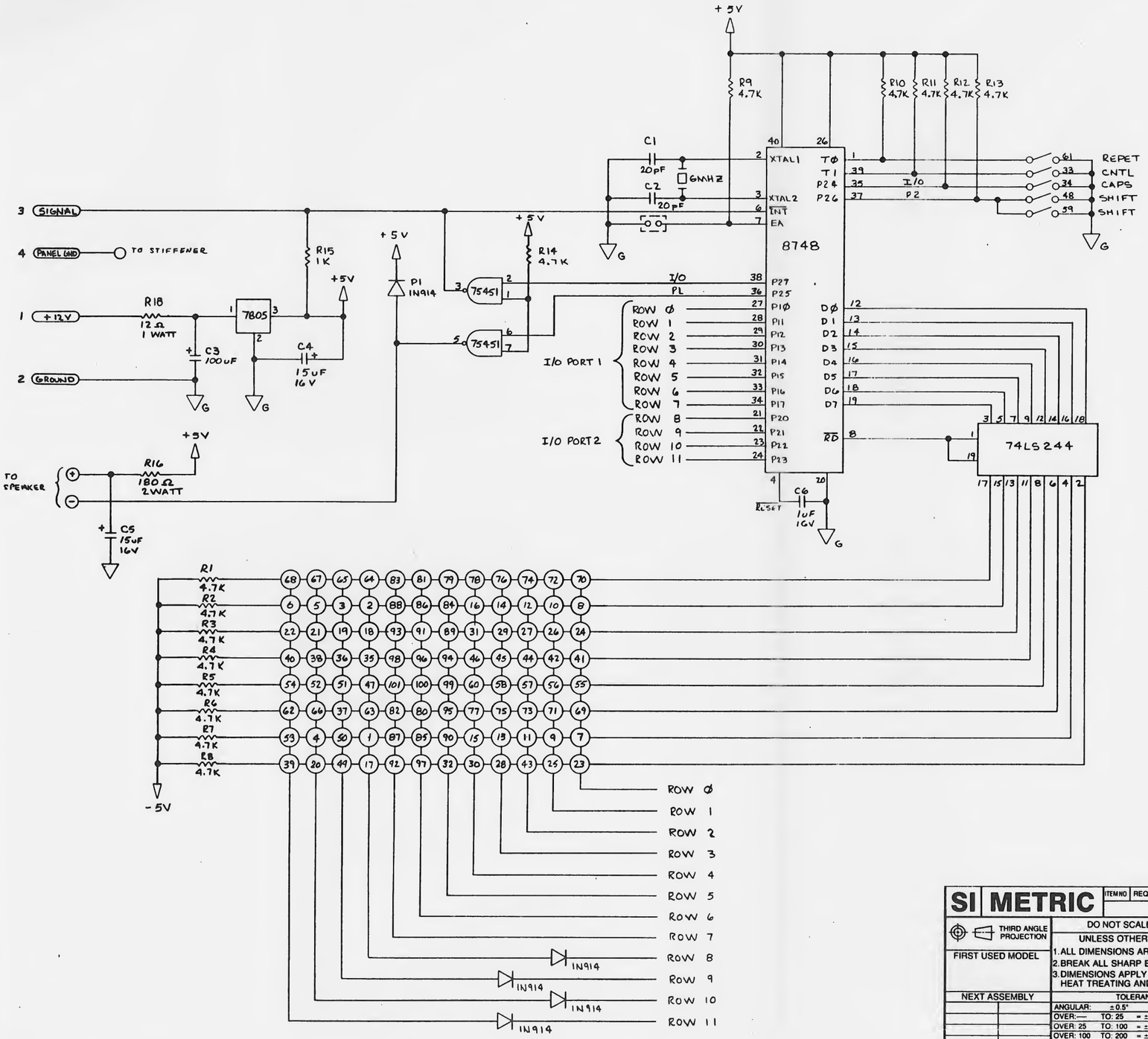
SCALE NONE SHEET 1 OF 1

BISHOP GRAPHICS ACCUPRESS REORDER NO. A35539

DWG. NO.		BM	REV.

REVISIONS

ZONE	LTR	DESCRIPTION	CHECK	DATE	APPROVED
	A	INITIAL RELEASE	J SINN	2/20/86	



ITEM NO	REQD	PART NUMBER	DESCRIPTION	MATL SPEC	REF DES	CODE IDENT

LIST OF MATERIALS

SI METRIC

THIRD ANGLE PROJECTION

FIRST USED MODEL

NEXT ASSEMBLY

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TOLERANCES:

ANGULAR:	±0.5°		
OVER: —	TO: 25	= ±0.2	(.008)
OVER: 25	TO: 100	= ±0.3	(.012)
OVER: 100	TO: 200	= ±0.5	(.020)
OVER: 200	TO: 300	= ±0.7	(.028)
OVER: 300	TO: 500	= ±0.9	(.035)
OVER: 500		= ±1	(.039)

DR	J. SINN	2/13/86
CHK		
APP		
APP		
APP		
MATL		
FINISH		

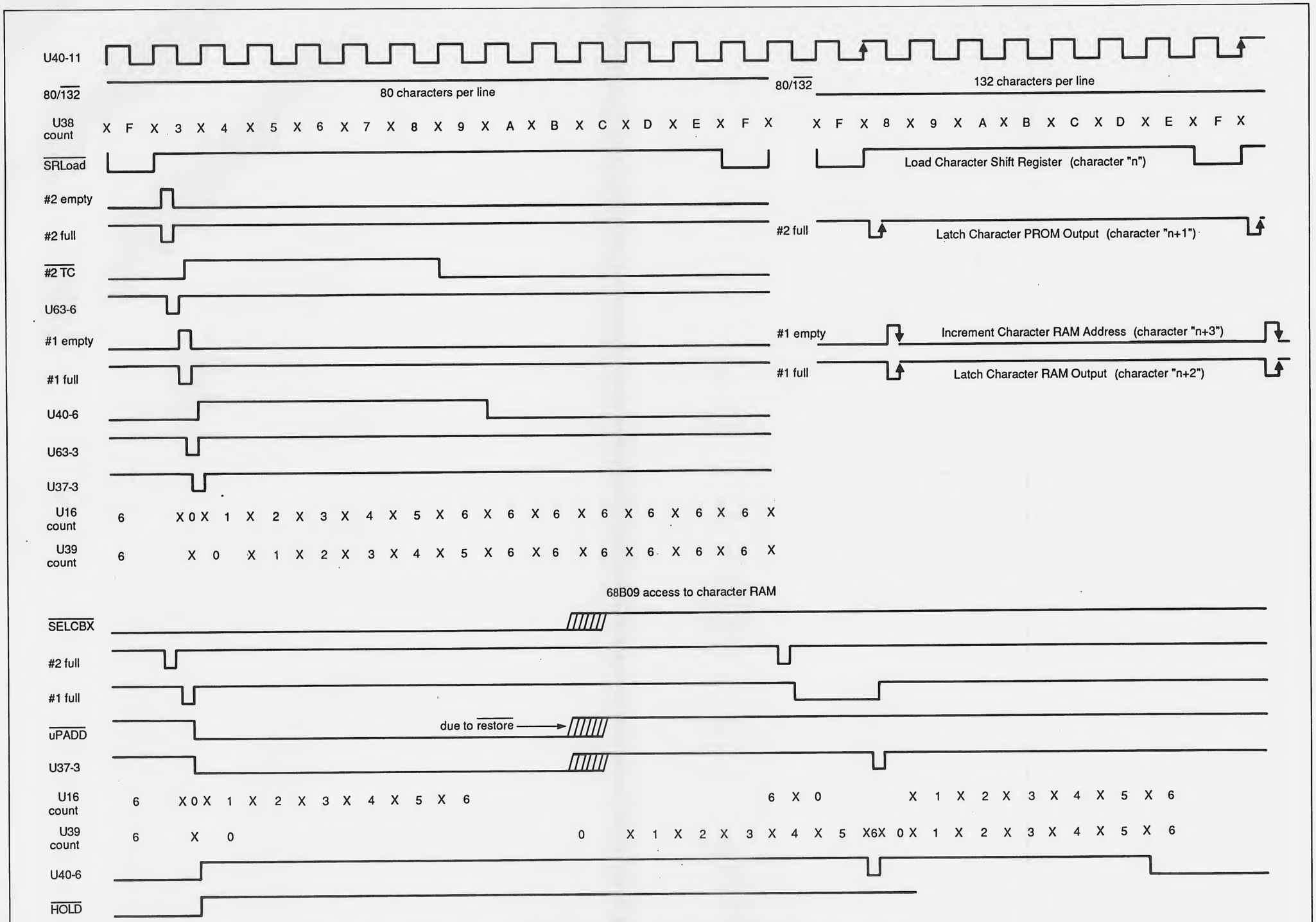
FARADAY

TITLE: KEYBOARD SCHEMATIC HIREZ - 100XL

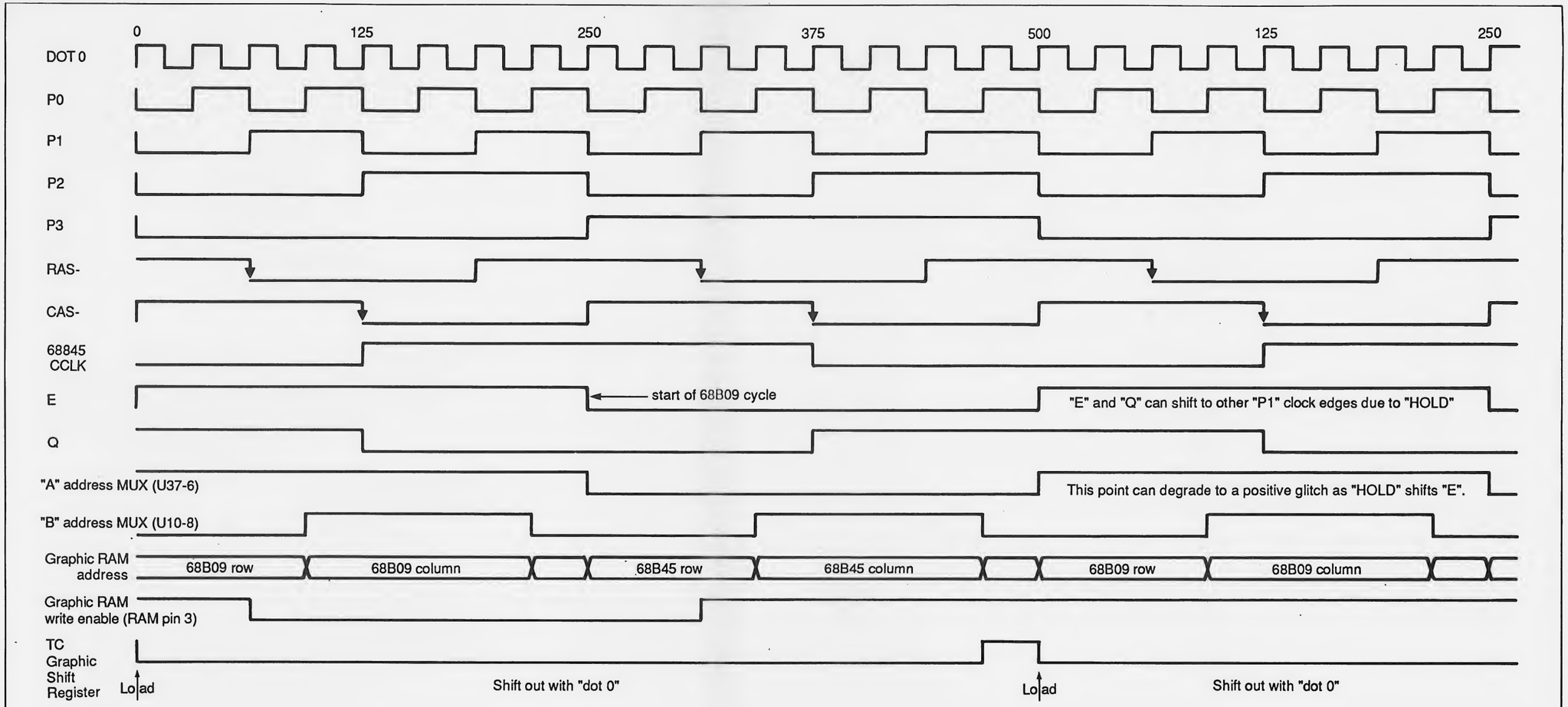
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D		01008900	A

SCALE NONE SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS RECORDER NO A3838



Character RAM Timing Diagram



Graphics RAM Timing Diagram